

# EE477L Fall 2018 Design Project#3 Report
## Digital Phase Locked-Loop (DPLL)

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## Contents

# 1 Introduction

A phase-locked loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors[1].

There are several different types of PLL, the simplest is an electronic circuit consisting of a variable frequency oscillator and a phase detector in a feedback loop, which is also we're going to build in this lab.

The oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal, then adjusting the oscillator to keep the phases matched. Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently, it can generate a frequency that is a multiple of the input frequency. These properties can be used for computer clock synchronization, demodulation, and frequency synthesis[2].

# 2 DPLL Individual Blocks

The circuit has five parts: phase frequency detector, charge pump, RC low-pass filter, voltage controlled oscillator and divide-by-10 divider block. In this part, the transistor-level circuit schematics and the description of each circuit will be given. For PFD, charge pump, VCO and divide-by-10 divider block, the physical layout and simulation will also be given.

## 2.1 Phase Frequency Detector (PFD)

### 2.1.1 Transistor-Level Circuit Schematics

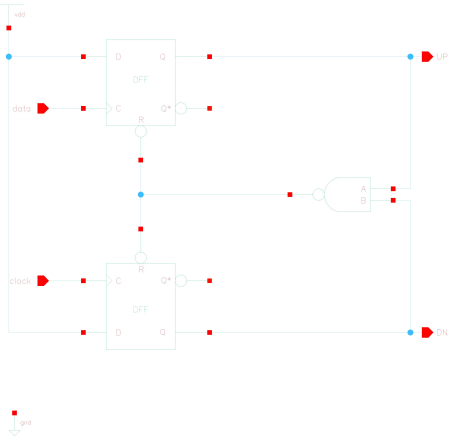


Figure 1: Schematics Circuit of Phase Frequency Detector

Figure 1 shows the schematics circuit of the Phase Frequency Detector.

### 2.1.2 Description of Circuit

A phase frequency detector (PFD) is an asynchronous circuit originally made of two D Flip-Flops. The logic determines which of the two signals has a zerocrossing earlier or more often. When used in a PLL application, lock can be achieved even when it is off frequency[3]. In a PLL, it can compare the input reference signal and the output of divide-by-10 circuit and give the UP and DN signal correspondingly when their frequencies are not matched.

### 2.1.3 Circuit-Level Simulations

Figure 2 shows the test circuit of the Phase Frequency Detector.

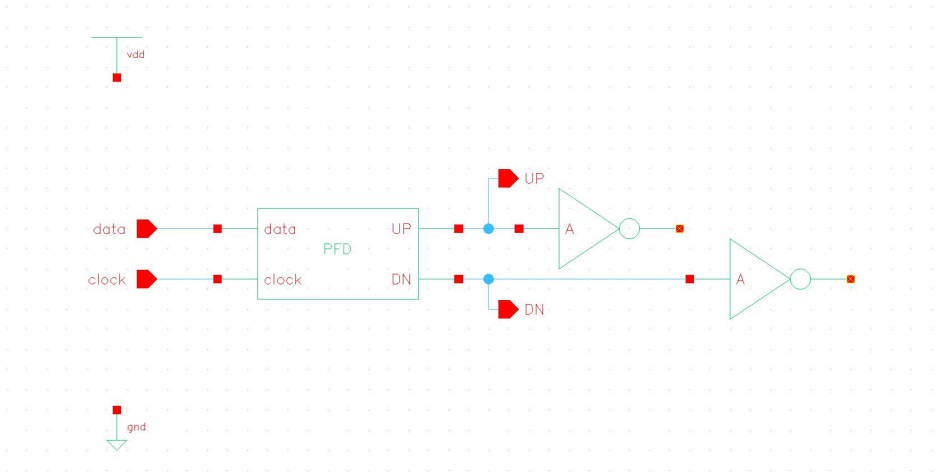


Figure 2: Schematics of Test Circuit of Phase Frequency Detector

### Identical Waveform

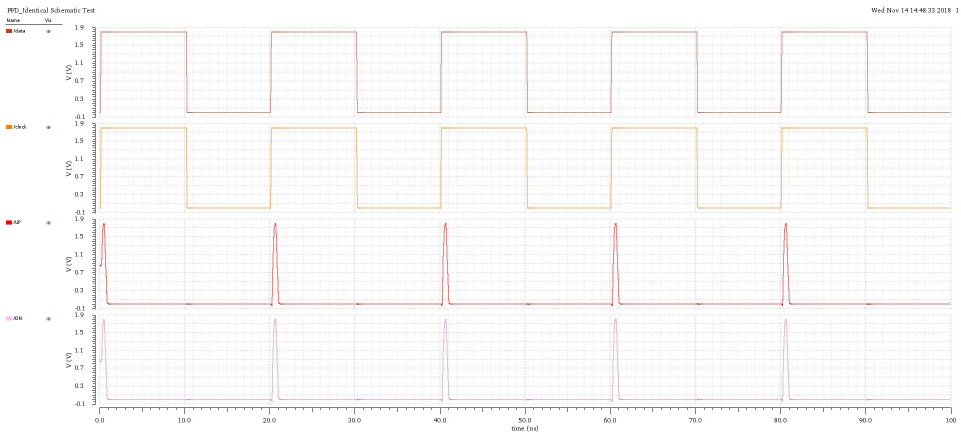

Figure 3: Test Result of Schematic PFD with Identical Inputs

Figure 3 shows the test result of schematics PFD when the two input have no difference. There are spikes at each rising edge of the input, it is inevitable because of the inner delay of the DFF and the NAND2.

### Data Lead Waveform

Figure 4 shows the test result of schematics PFD with data is lead to the clock.

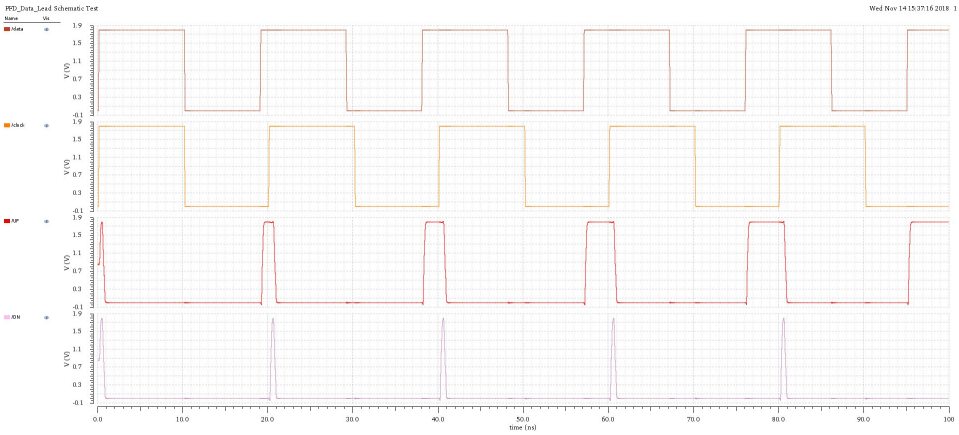

Figure 4: Test Result of Schematic PFD with Data Lead

### Data Lag Waveform

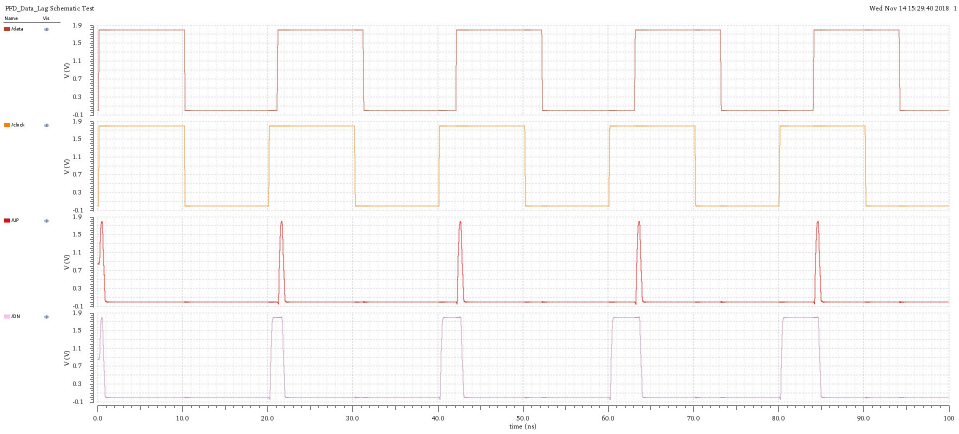

Figure 5: Test Result of Schematic PFD with Data Lag

Figure 5 shows the test result of schematics PFD with data is lag to the clock.

### 2.1.4 Physical Layout

Figure 6 shows the layout of PFD. The height of it is 19$\mu$m, and the width is 46.45$\mu$m.

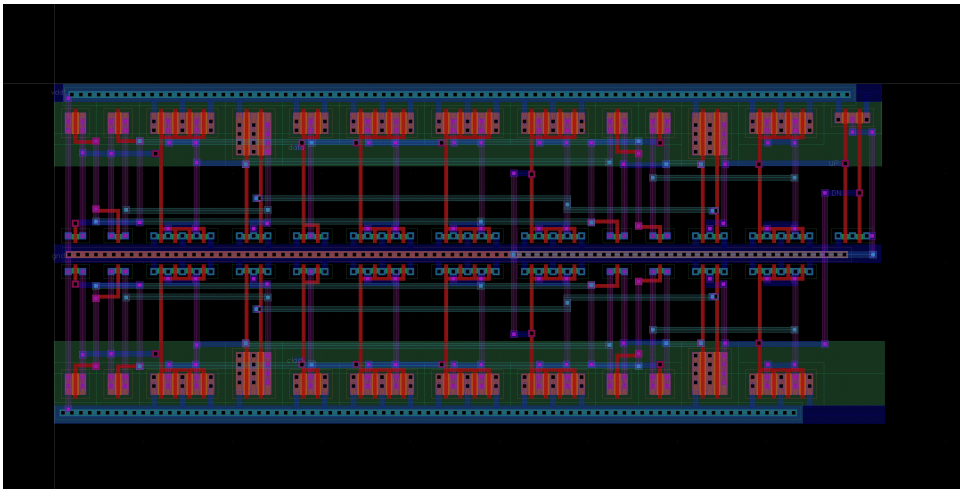

Figure 6: Layout of PFD

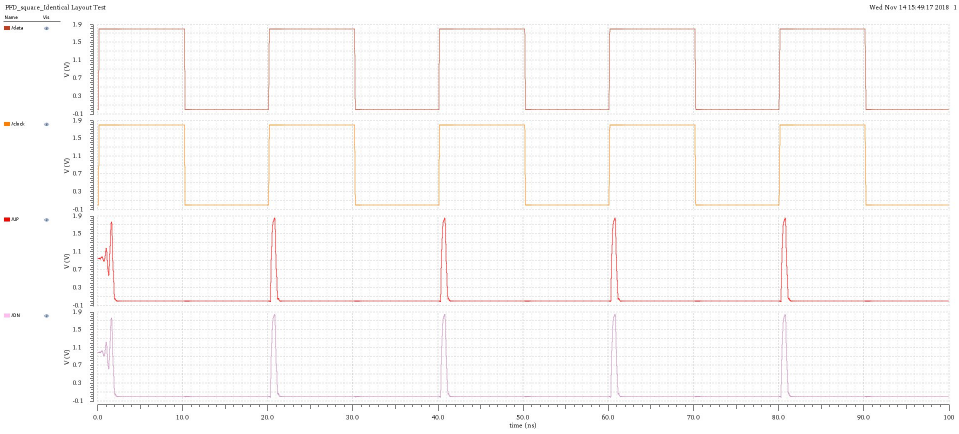


Figure 7: Test Result of Layout PFD with Identical Inputs

### 2.1.5 Layout Simulation

#### Identical Waveform

Figure 7 shows the test result of layout of PFD when the two input have no difference. There are still spikes at each rising edge of the input.

#### Data Lead Waveform

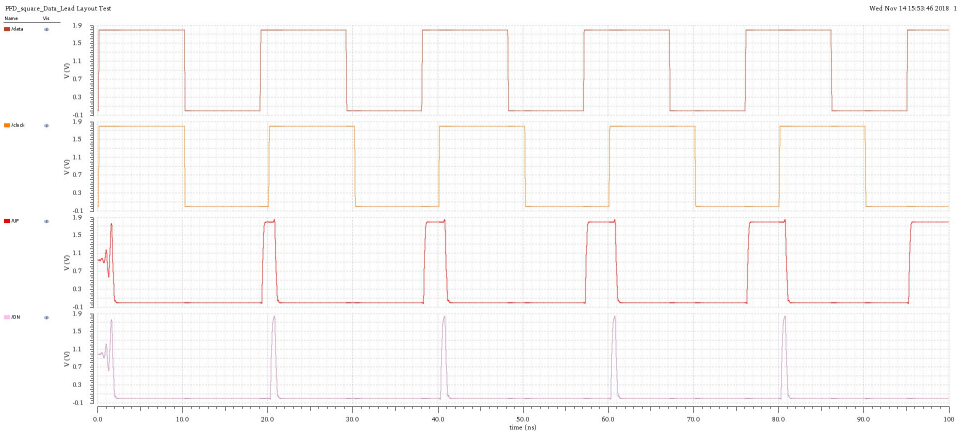

Figure 8: Test Result of Layout PFD with Data Lead

Figure 8 shows the test result of layout of PFD with data is lead to the clock.

#### Data Lag Waveform

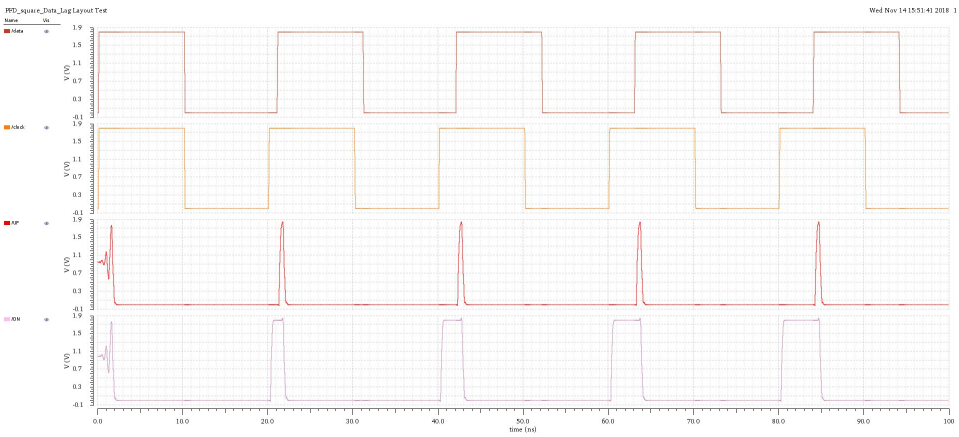

Figure 9: Test Result of Layout PFD with Data Lag

Figure 9 shows the test result of layout of PFD with data is lag to the clock.

### 2.1.6 Layout vs. Schematics (LVS) Result

The LVS result is given in the LVS directory.

## 2.2 Charge Pump

A charge pump has a sub-block as 50%-Crossing Special Switch, which is working as a switch and controlling if the input can be transferred to the output.

**50%-Crossing Special Switch**

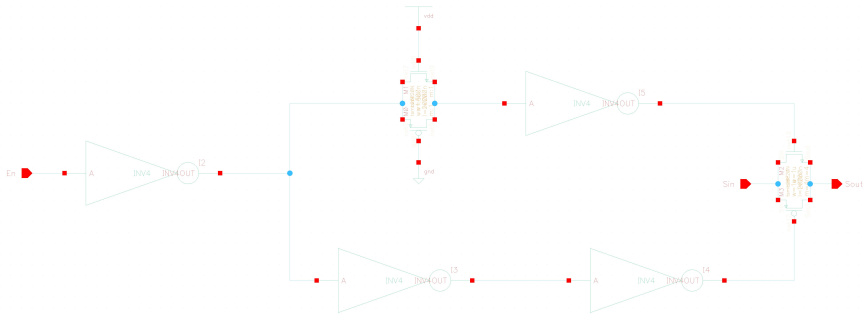

Figure 10: Schematics Circuit of 50%-Crossing Special Switch

Figure 10 shows the schematics circuit of the 50%-crossing special switch.

**Charge Pump**

### 2.2.1 Transistor-Level Circuit Schematics

Figure 11 shows the schematics circuit of the charge pump.

### 2.2.2 Description of Circuit

A charge pump is for charging the output loop filter which can provide a stable voltage bias to the voltage controlled oscillator. For the charge

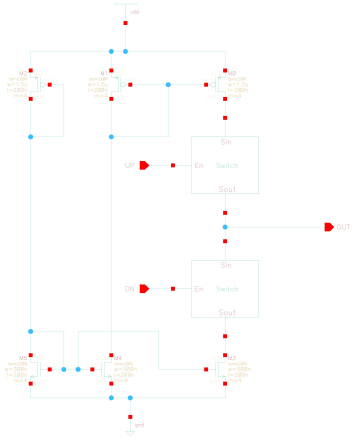


Figure 11: Schematics Circuit of Charge Pump

pump, when the UP signal is turned on, the source current will charge-up the output load capacitor and when DN signal is turned on, the output load will discharge. So when the UP and DN signal is balanced, say the input of phase frequency detector has no difference, then the output load will have a constant voltage bias.

### 2.2.3 Circuit-Level Simulations

#### 50%-Crossing Special Switch

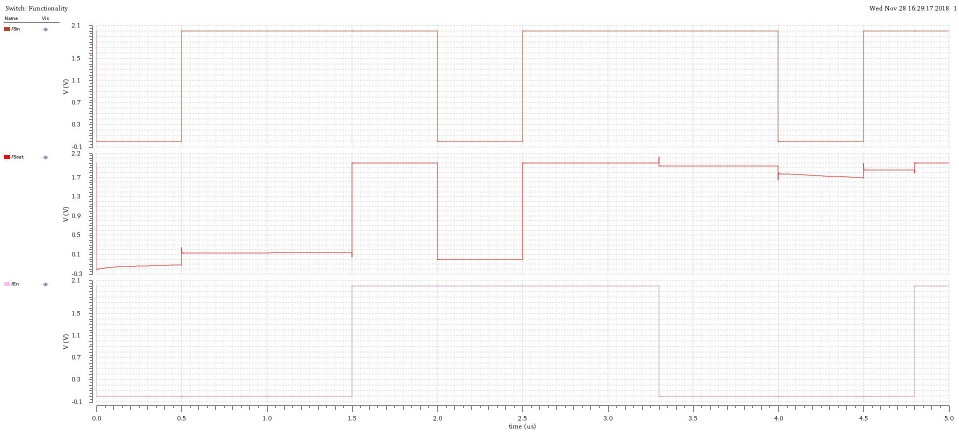


Figure 12: Test Result of 50%-Crossing Special Switch Functionality

Figure 12 shows the test result of functionality of the 50%-crossing special switch. Only when EN is on, the input signal can be transferred to

the output.

### Charge Pump

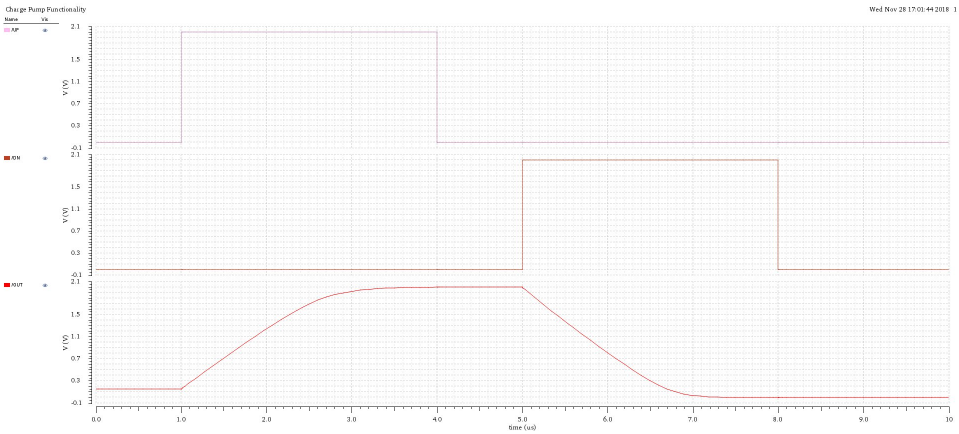


Figure 13: Test Result of Charge Pump Functionality

Figure 13 shows the test result of functionality of the charge pump. When the input UP is high, the output load is charging and when DN is high, the output load will discharge. The charging time and discharging velocity is almost the same so the charge pump is a balanced device.

#### 2.2.4 Physical Layout

### 50%-Crossing Special Switch

Figure 14 shows the layout of the 50%-crossing special switch. The height of it is 10$\mu$m, and the width is 26.40$\mu$m.

### Charge Pump

Figure 15 shows the layout of the charge pump. The height of it is 19$\mu$m, and the width is 40.85$\mu$m.

#### 2.2.5 Layout Simulation

### 50%-Crossing Special Switch

Figure 16 shows the test result functionality of layout of the 50%-crossing special switch.

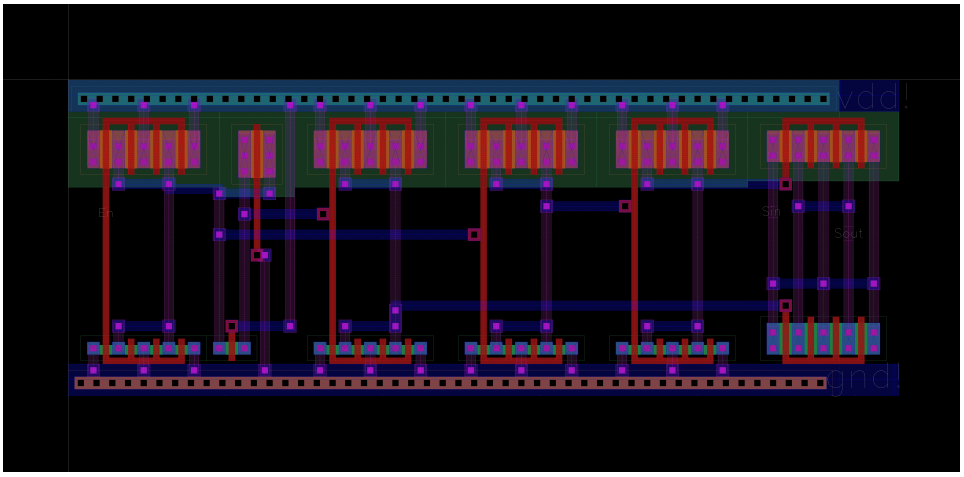


Figure 14: Layout of 50%-Crossing Special Switch

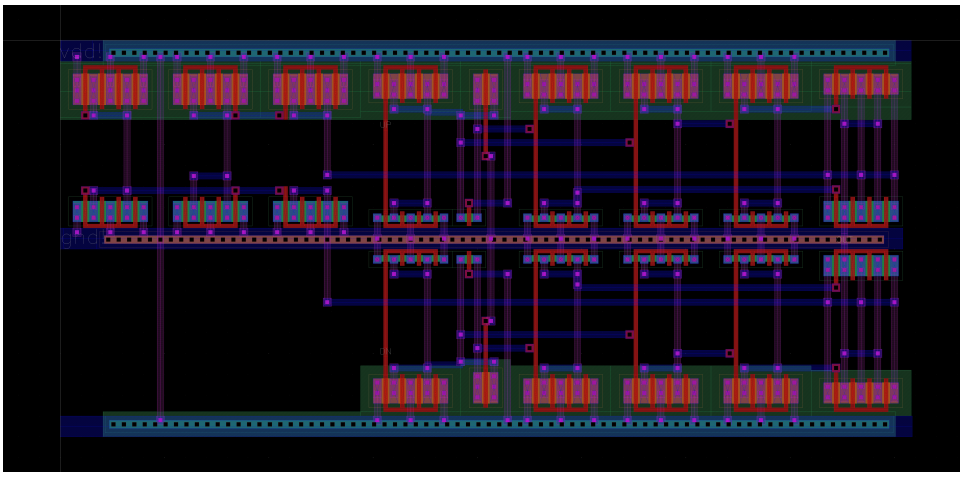


Figure 15: Layout of Charge Pump

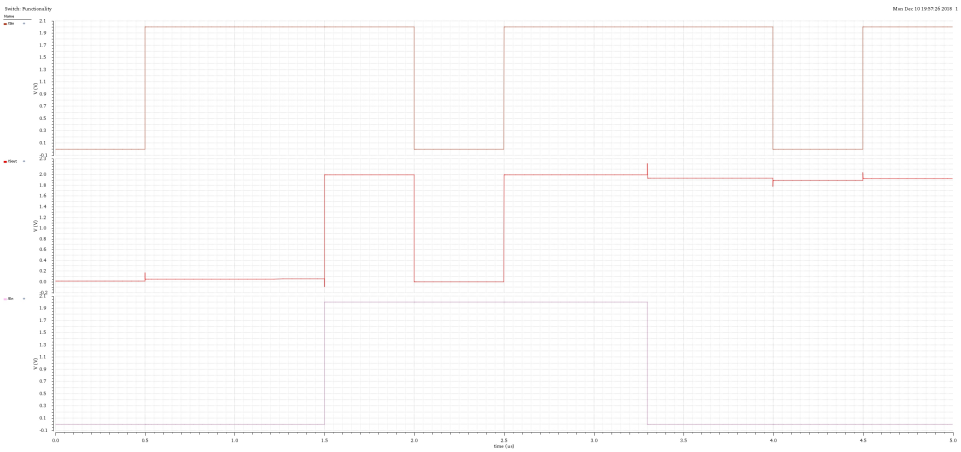

Figure 16: Test Result of Layout of 50%-Crossing Special Switch Functionality

### Charge Pump

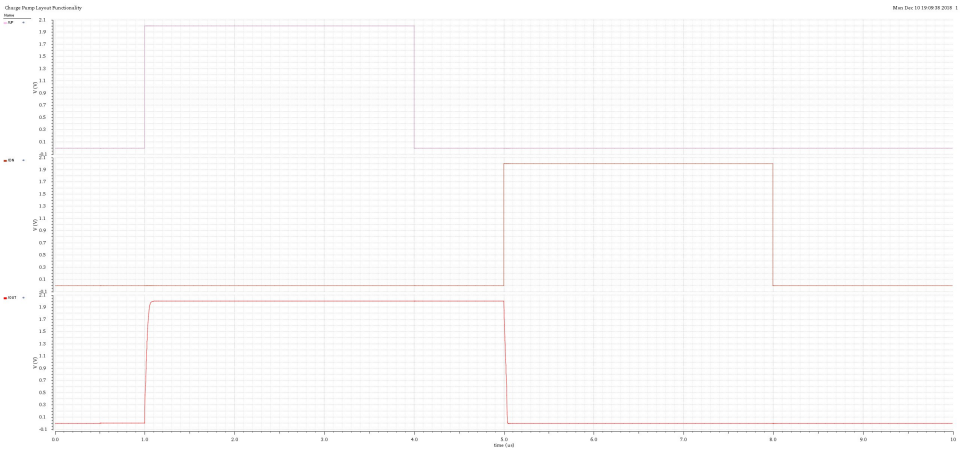

Figure 17: Test Result of Layout of Charge Pump Functionality

Figure 17 shows the test result functionality of layout of the charge pump. The charge and discharge curves are different from the schematics one, it is because the output load is different for the two cases. For the schematics case, the output load is a huge capacitor with 100pF, however for the layout case, the capacitor used is the same as the one used in DPLL, which is only in fF level. That's the reason that the charging and discharging time is much faster than then schematics case.

### 2.2.6 Layout vs. Schematics (LVS) Result

The LVS result is given in the LVS directory.

## 2.3 RC Low-Pass Filter (Loop Filter)

### 2.3.1 Transistor-Level Circuit Schematics

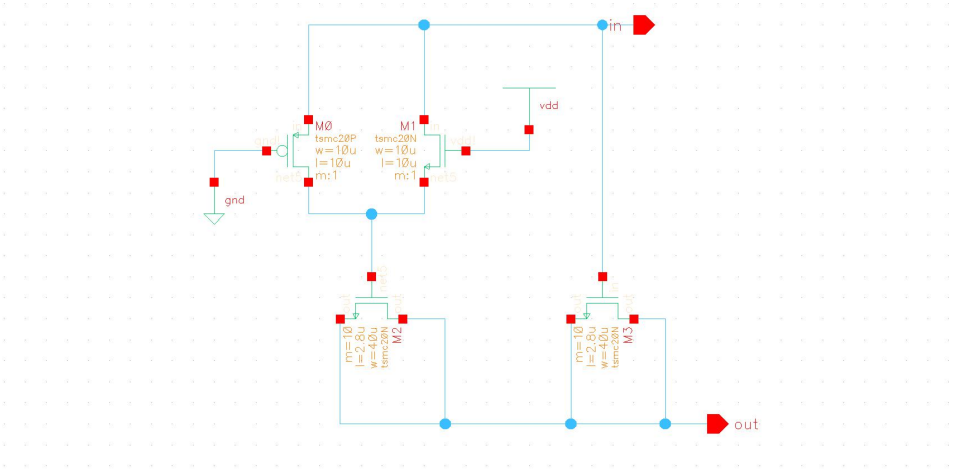


Figure 18: Schematics Circuit of RC Low-Pass Filter

Figure 18 shows the schematics circuit of the RC low-pass filter.

### 2.3.2 Description of Circuit

The loop filter is a RC low-pass filter, which is used for stabilizing the output signal of the charge pump. Since the input signal UP and DN to the charge pump is very unstable, and also its output is very sensitive to the input, it will be very unstable. However, the input provided to the input of the voltage controlled oscillator should be a stable one. Then there need a low-pass filter to eliminate the spikes of the output of charge pump and make it more smooth and stable.

## 2.4 Voltage Controlled Oscillator (VCO)

### 2.4.1 Transistor-Level Circuit Schematics

Figure 19 shows the schematics circuit of the voltage controlled oscillator.

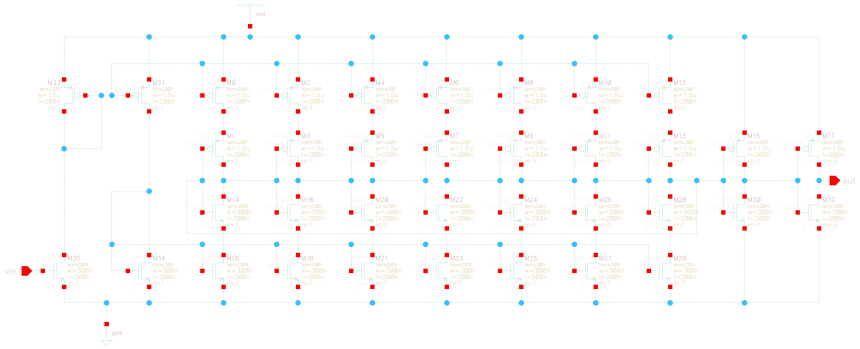

Figure 19: Schematics Circuit of Voltage Controlled Oscillator

### 2.4.2 Description of Circuit

The VCO block is the main part in the PLL that produces the output clock signal. The input of a VCO is a voltage bias and the output of it will be a clock signal with specific frequency and that frequency is determined by the input voltage bias.

As shown in Figure 19,the oscillating part is the ring oscillator. So the factors that will affect the output frequency is the number of stages and the current go through the inverter. Then we have the frequency equation as Equation 1 and 2:

$$f_{osc} = K \times \frac{I_D}{N},\ K = \frac{1}{C_{totao} \times V_{DD}} \tag{1}$$

$K$ is a constant, and since the current $I_D$ go through the MOSFET is defined as (ignore channel length modulation):

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{th})^2 \tag{2}$$

Then controlling the input of voltage bias $V_{in}$ can control the frequency of output clock.

### 2.4.3 Circuit-Level Simulations

#### Functionality Test

Figure 20 shows the test result of the VCO when the input signal is a step function.

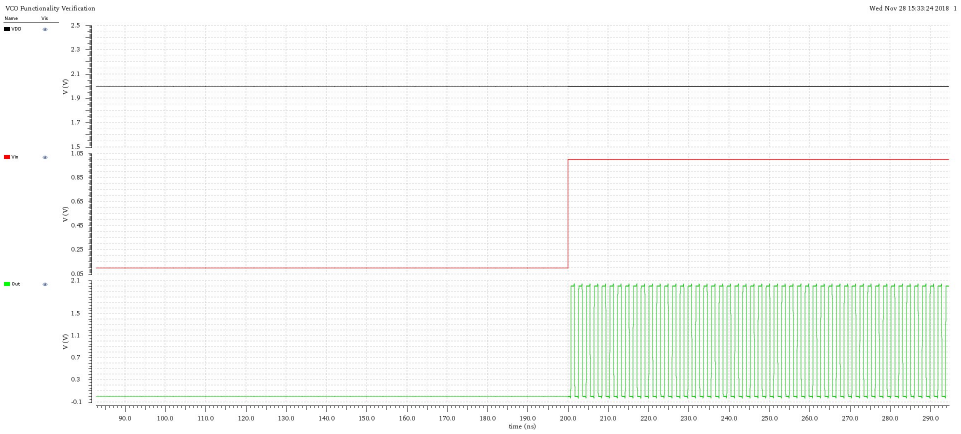


Figure 20: Test Result of Voltage Controlled Oscillator with Step Input

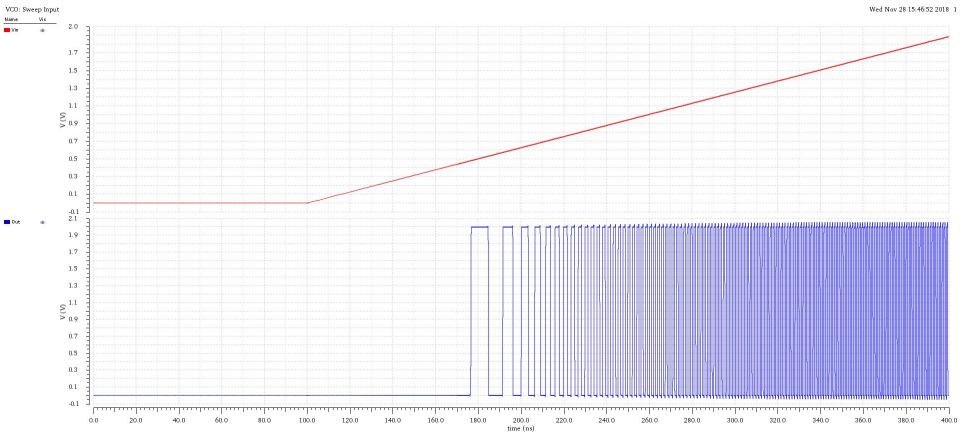


Figure 21: Test Result of Voltage Controlled Oscillator with Sweep Input

Figure 21 shows the test result of the VCO when the input signal is a sweep function.

### Period Measurement

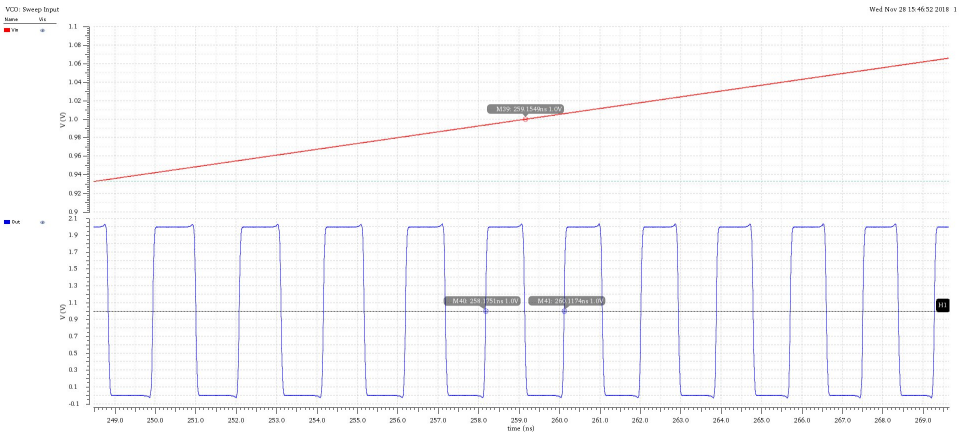

Figure 22: Test Result of Voltage Controlled Oscillator Output Period

Figure 22 shows the test result of the VCO output period when the input is 1V. The period is about 1.95ns, then the frequency is about 514.9MHz.

### Step Function Supply Response

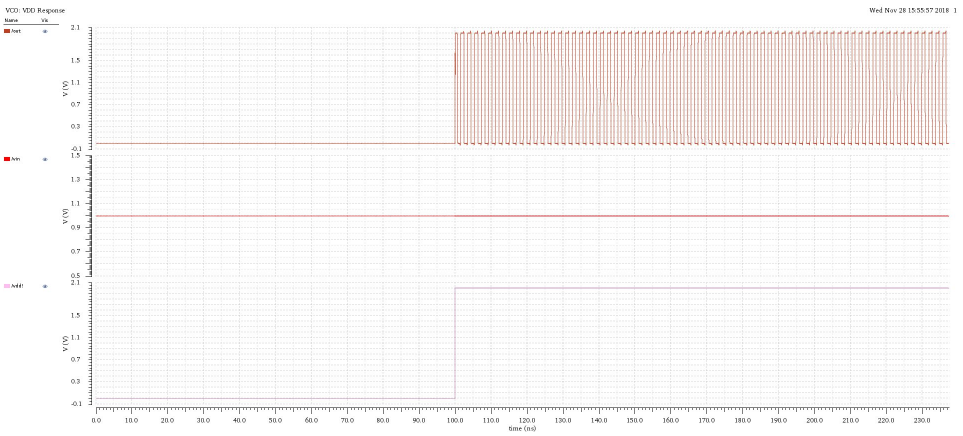

Figure 23: Test Result of Voltage Controlled Oscillator with Step Supply

Figure 23 shows the test result of the VCO when the supply signal is a step function.

### 2.4.4 Physical Layout

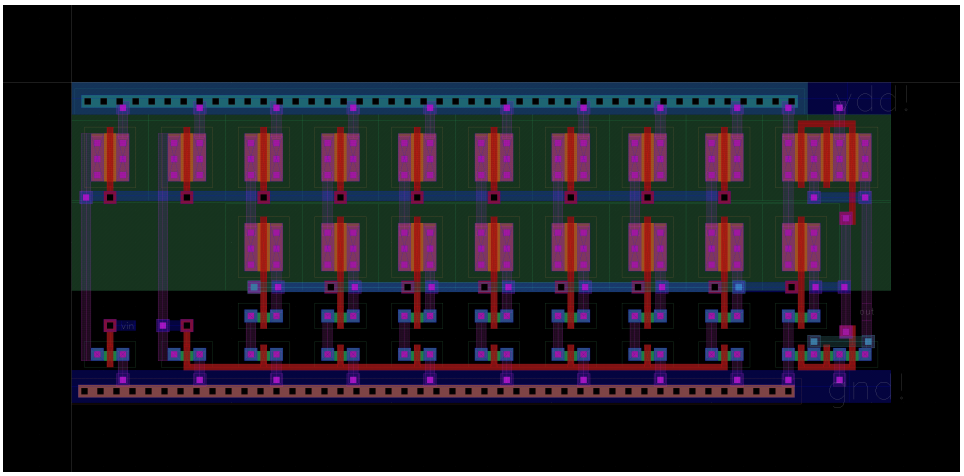


Figure 24: Layout of Voltage Controlled Oscillator

Figure 24 shows the layout of the VCO. The height of it is 10$\mu$m, and the width is 25.60$\mu$m.

### 2.4.5 Layout Simulation

**Functionality Test**

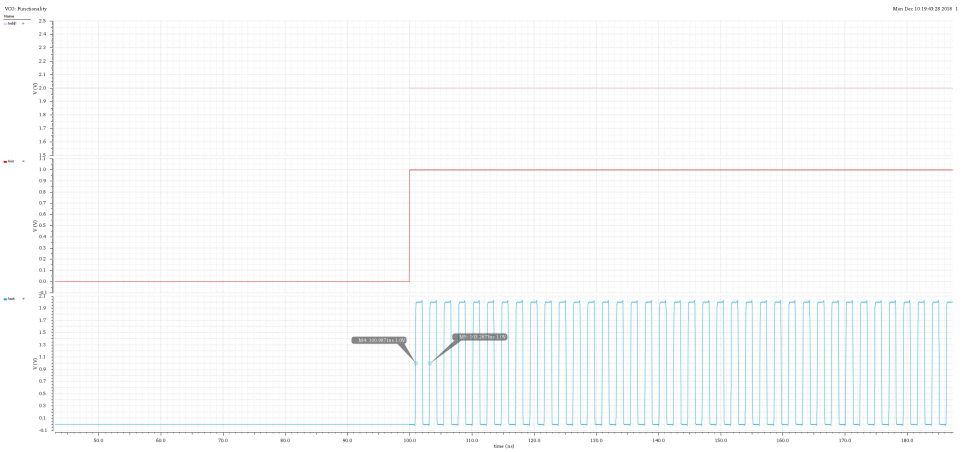

Figure 25: Test Result of Layout of Voltage Controlled Oscillator with Step Input

Figure 25 shows the test result of the layout of VCO when the input signal is a step function.

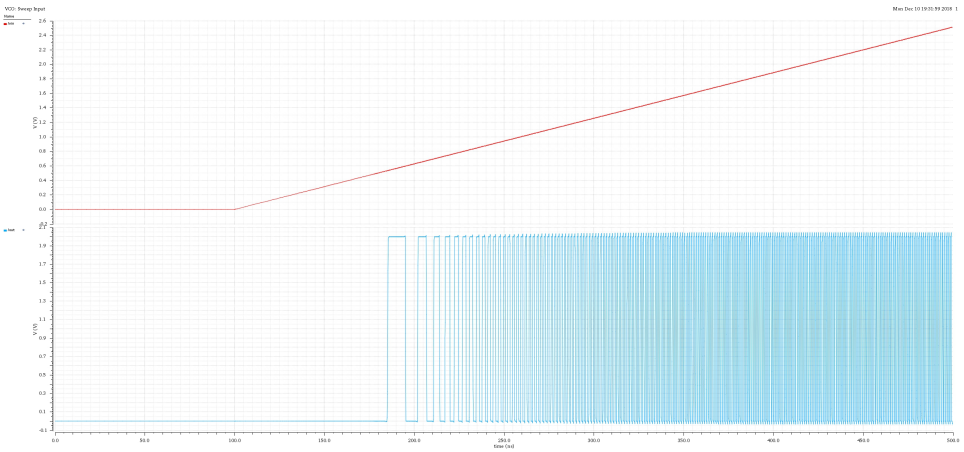

Figure 26: Test Result of Layout of Voltage Controlled Oscillator with Sweep Input

Figure 26 shows the test result of the layout of VCO when the input signal is a sweep function.

**Period Measurement**

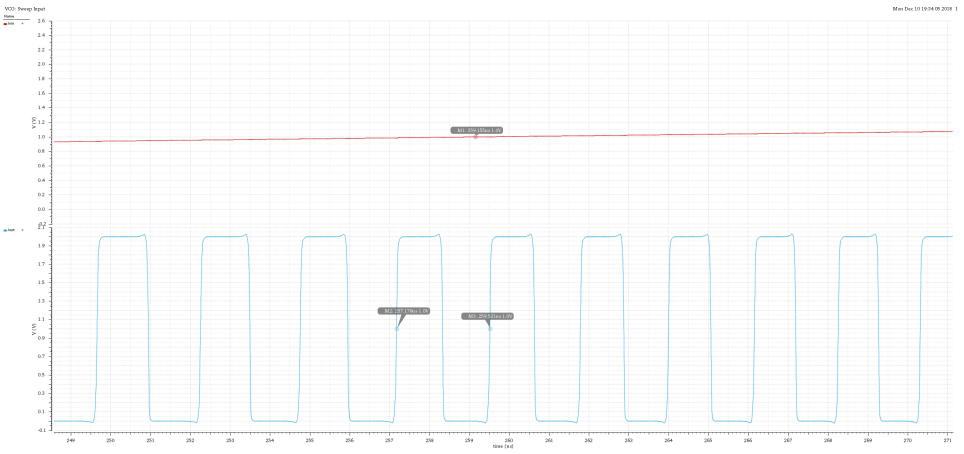

Figure 27: Test Result of Layout of Voltage Controlled Oscillator Output Period

Figure 27 shows the test result of the layout of VCO output period when the input is 1V. The period is about 2.34ns, then the frequency is about 427.0MHz. This frequency is smaller than it in schematics, it is because the parasitic of capacitors in wires are taken into account, which means it will take more time to charge all the parasitic capacitors, which slow down the

frequency.

**Step Function Supply Response**

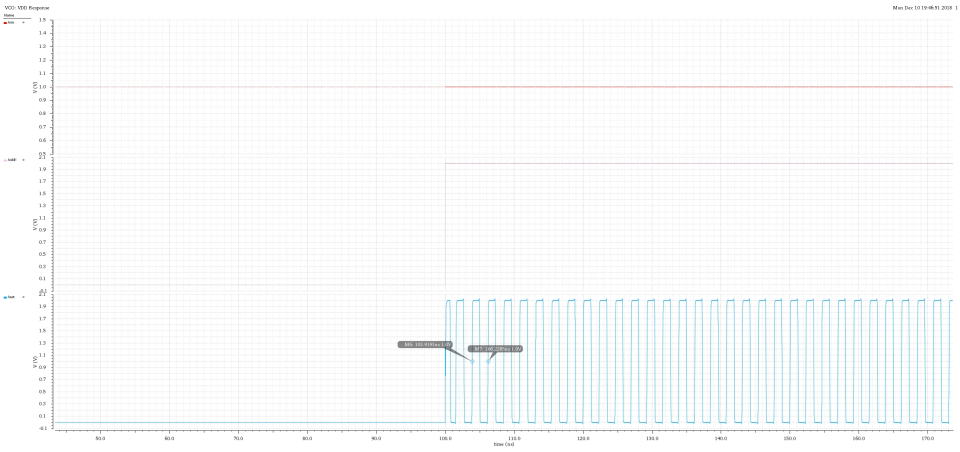

Figure 28: Test Result of Layout of Voltage Controlled Oscillator with Step Supply

Figure 28 shows the test result of the layout of VCO when the supply signal is a step function.

### 2.4.6 Layout vs. Schematics (LVS) Result

The LVS result is given in the LVS directory.

## 2.5 Divide-by-10 Divider Block (DIV)

### 2.5.1 Transistor-Level Circuit Schematics

Figure 29 shows the schematics circuit of the divide-by-10 divider block.

### 2.5.2 Description of Circuit

A divide-by-10 divider block can generate the output signal with the frequency precisely $\frac{1}{10}$ as the input signal. Then the output signal can be used as the input of the phase frequency detector. The precision of the divide-by-10 circuit will also decide the accuracy of the frequency of output signal.

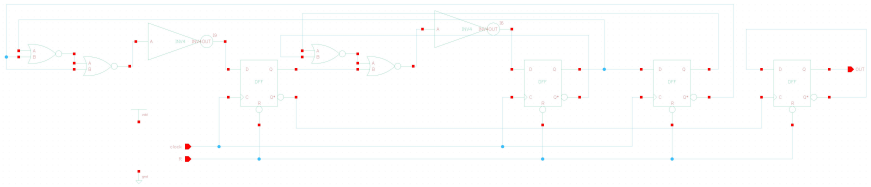

Figure 29: Schematics Circuit of Divide-by-10 Divider Block

### 2.5.3 Circuit-Level Simulations

#### 100MHz Performance

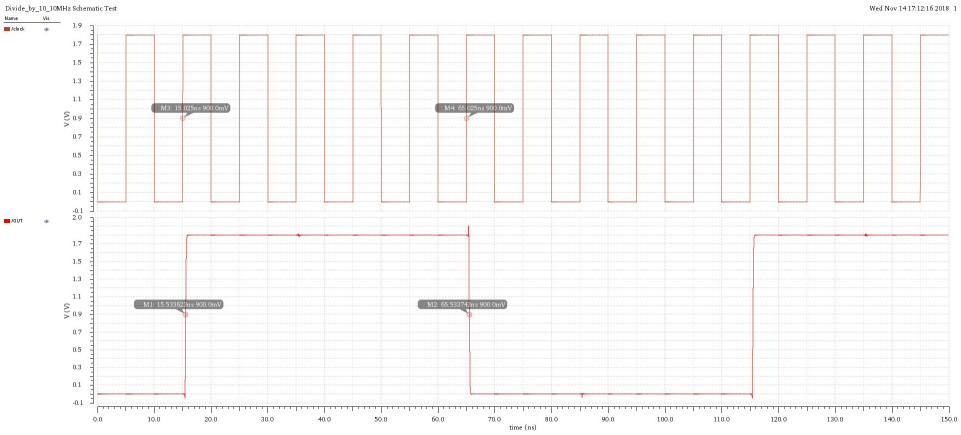


Figure 30: Test Result of Divide-by-10 Divider Block with 100MHz Input

Figure 30 shows the test result of schematics divide-by-10 divider block with 100MHz input, the 50% rising edge delay $t_{rise}$ is 508.6ps,and the 50% falling edge delay $t_{fall}$ is 508.7ps.

#### Maximum Frequency

Figure 31 shows the test result of schematic divide-by-10 divider block. The definition of functioning in this case is that the 90% point of the rising

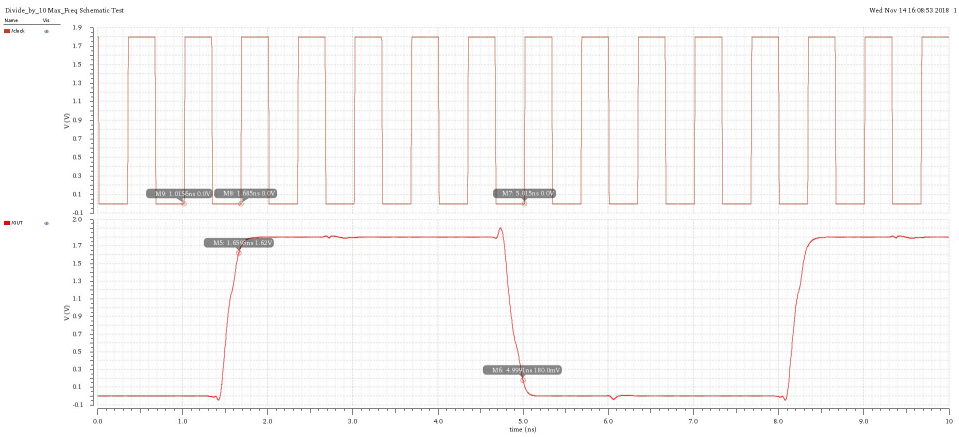


Figure 31: Test Result of Divide-by-10 Divider Block with Maximum Frequency

edge and the 10% point of the falling edge is right before than next rising edge of the clock. Base on this condition, the maximum frequency is about 1.5GHz.

### 2.5.4 Physical Layout

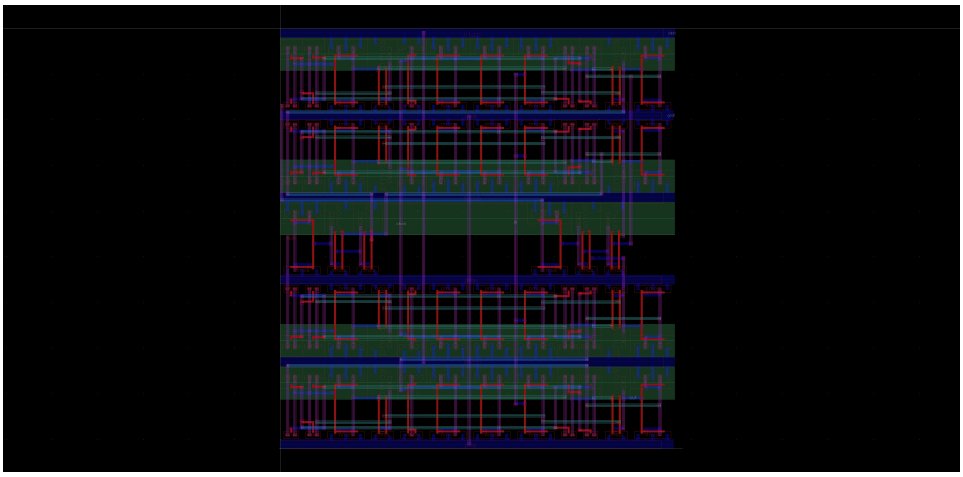

Figure 32: Layout of Divide-by-10 Divider Block

Figure 32 shows the layout of divide-by-10 divider block. The height of the it is 46$\mu$m, and the width is 43.2$\mu$m.

### 2.5.5 Layout Simulation

#### 100MHz Performance

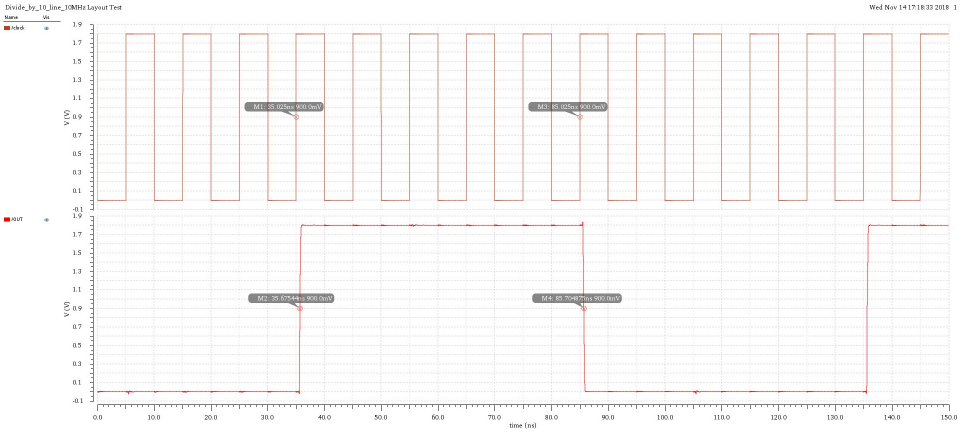

Figure 33: Test Result of layout of Divide-by-10 Divider Block with 100MHz Input

Figure 33 shows the test result of layout of divide-by-10 divider block with 100MHz input, the 50% rising edge delay $t_{rise}$ is 648.6ps,and the 50% falling edge delay $t_{fall}$ is 679.8ps.

#### Maximum Frequency

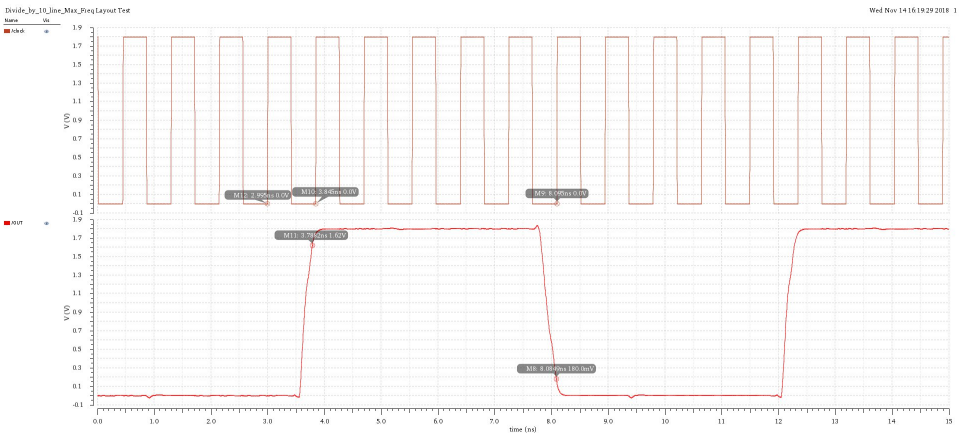

Figure 34: Test Result of Layout of Divide-by-10 Divider Block with Maximum Frequency

Figure 34 shows the test result of layout of divide-by-10 divider block.

The maximum frequency is about 1.18GHz.

### 2.5.6 Layout vs. Schematics (LVS) Result

The LVS result is given in the LVS directory.

# 3 Digital PLL System

## 3.1 Block Level Schematics of Entire DPLL

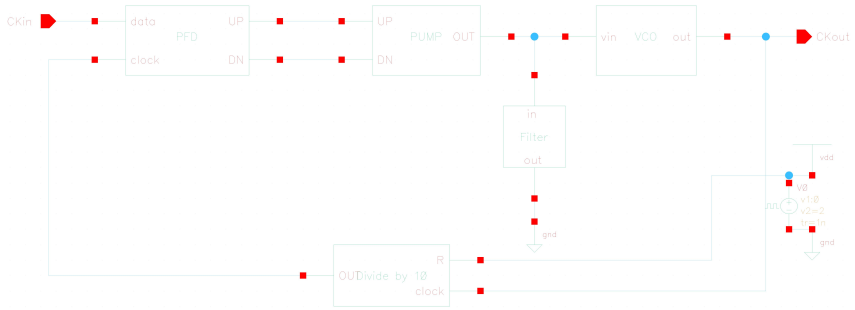


Figure 35: Schematics Circuit of Entire DPLL

Figure 35 shows the schematics circuit of the entire digital phase locked-loop.

## 3.2 Description of Circuit

As shown in Figure 35, a DPLL has five parts. Phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO) and divide-by-10 divider block. The input of PFD is the reference signal and the output of divide-by-10 divider block. When there is difference between them, an UP or DN signal will be generated. The UP and DN signal will be capture by the charge pump to charge the output load capacitor. The loop filter is for stabilizing the output of the charge pump and provide a smooth and stable voltage bias to the VCO. With a stable voltage input, the VCO will generate a stable clock signal with a frequency as 10 times to the input reference signal.

## 3.3 Circuit Level Simulations

### 3.3.1 Lock Time

Figure 36 shows the test result of DPLL. At t=2$\mu$s, the signal is stable, then the lock time is around 1$\mu$s. The VCO input is around 978.5mV. And

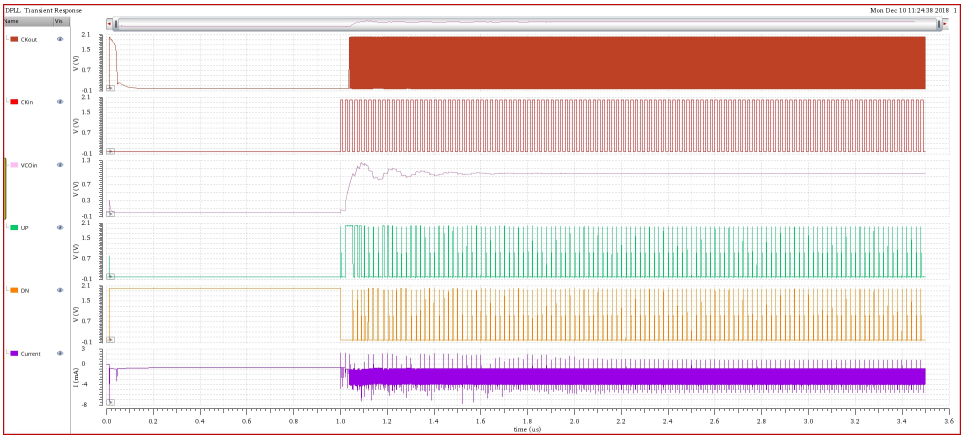


Figure 36: Test Result of DPLL Lock Time

the current consumption is about 1.204mA, so the power consumption is about 2.408mW.

### 3.3.2 Output Period

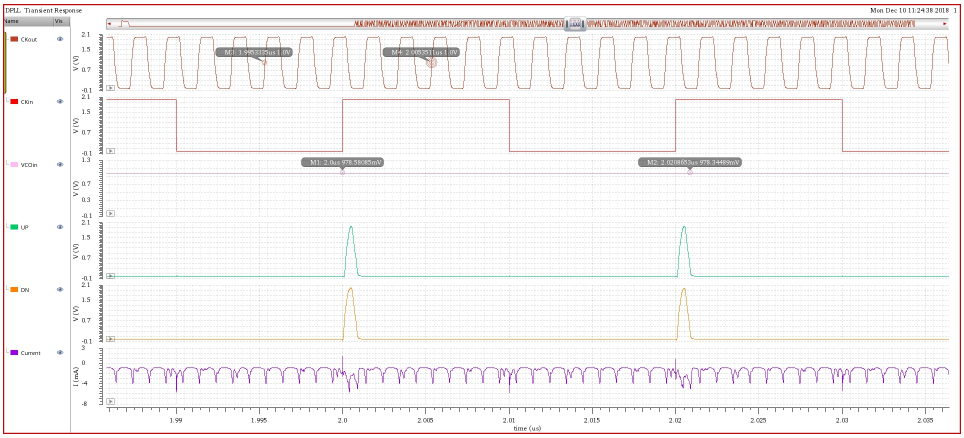


Figure 37: Test Result of DPLL Output Period

Figure 37 shows the test result of DPLL after the signal is stable. At t=2$\mu$s, the signal is stable. And at that time point, the period of the output signal is about 2.004ns, then the output frequency is about 499.12MHz.

## 3.4 Physical Layout

Figure 38 shows the layout of DPLL. The height of it is 64$\mu$m, and the width is 113.25$\mu$m.

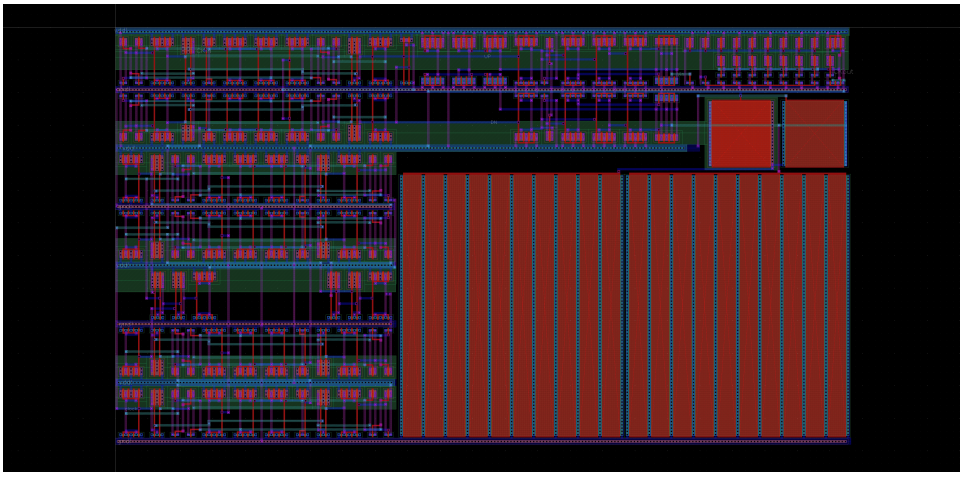

Figure 38: Layout of Entire DPLL

## 3.5 Layout Level Simulations

### 3.5.1 Lock Time

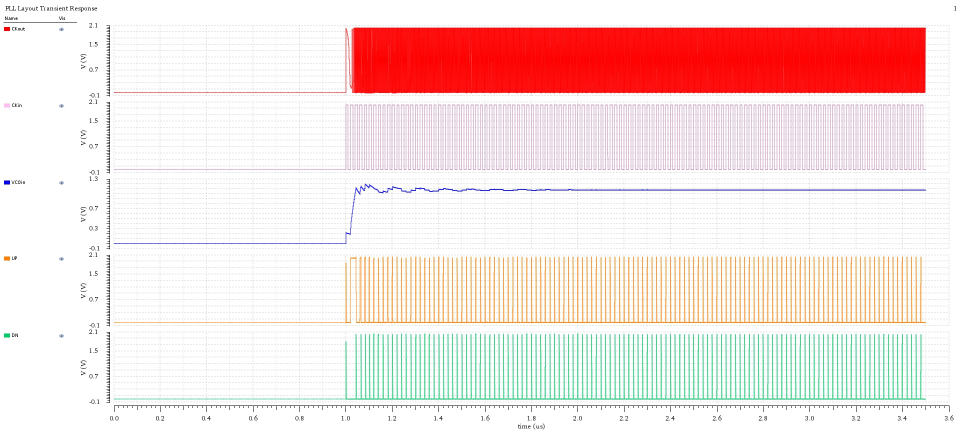

Figure 39: Test Result of Layout of DPLL Lock Time

Figure 39 shows the test result of layout of DPLL. At t=2.1$\mu$s, the signal is stable, then the lock time is around 1.1$\mu$s. The VCO input is around 1.075V.

### 3.5.2 Output Period

Figure 40 shows the test result of layout of DPLL after the signal is stable. At t=2.1$\mu$s, the signal is stable. And at that time point, the period

Figure 40: Test Result of Layout of DPLL Output Period

of the output signal is about 1.9997ns, then the output frequency is about 500.09MHz.

### 3.5.3 Power

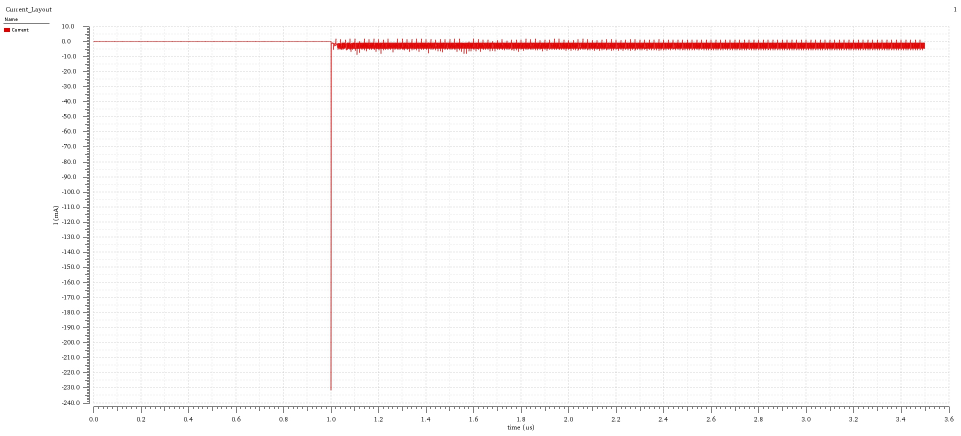

Figure 41: Test Result of Layout DPLL Output Power

Figure 41 shows the test result of layout of DPLL of current consumption. And the current consumption is about 2.024mA, so the power consumption is about 4.048mW.

## 3.6 Layout vs. Schematics (LVS) Result

The LVS result is given in the LVS directory.

## 3.7 Optimization: Minimize=Area×Power×Lock Time

### 3.7.1 Optimization Concept

#### Charge Pump Optimization

For charge pump, I increased the size of the current mirror so that the current generated get larger and can charge and discharge the capacitor quicker, which will lead to a faster lock time. And it will not effect the power consumption that much since this current is quite small compared with the current in VCO.

#### Loop Filter Optimization

For the loop filter, it should works like a large resistor series with a huge capacitor so that it has a large time constant, which will lead to a lower frequency. Since the capacitor will take a lot of area in the layout, I tried to decreased it and increased the value of resistor as a compensation so that the time constant will not change so much. And what's more, if the time constant is kind of small, although the stability of the circuit will be affected, the charge time will be much faster than a large capacitor, which means the lock time is faster for a decent small capacitor. Figure 42 shows the

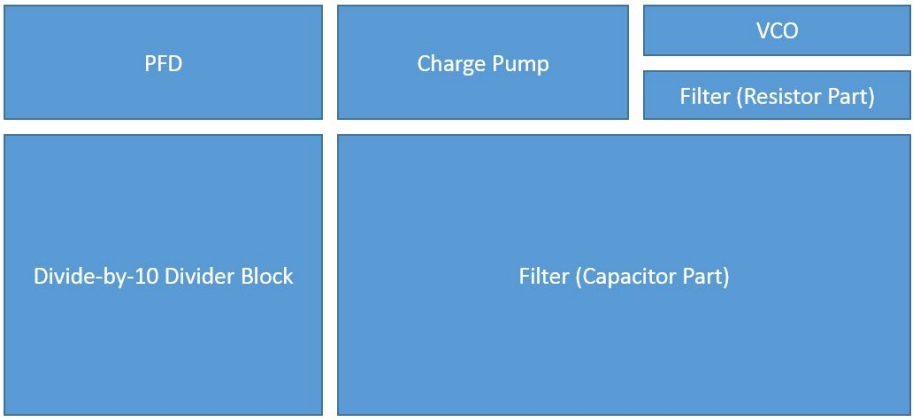


Figure 42: Layout of Blocks Circuit

layout of blocks circuit, which will have a better usage efficiency of area.

### 3.7.2 Optimization Result

The optimization result of the layout of DPLL is 32273.89 ($\mu m^2 \times mW \times \mu s$). Table1 shows the simulation result of DPLL.

Table 1: Simulation Result of DPLL

| **Parameters** | **Schematics** | **Layout** |
|---|---|---|
| Area $(\mu m \times \mu m)$ | N/A | 7248 |
| Power Consumption $(mW)$ | 2.048 | 4.048 |
| Lock Time $(\mu s)$ | 1 | 1.1 |

## References

**1.** R. Best. *Phase Locked Loops 6/e : Design, Simulation, and Applications: Design, Simulation, and Applications*. Mcgraw-hill, 2007.

**2.** W.F. Egan. *Phase-Lock Basics*. Wiley - IEEE. Wiley, 2007.

**3.** P. Horowitz and W. Hill. *The Art of Electronics*. Cambridge University Press, 2015.