EE479L Fall 2018 Design Project#1 Report
CMOS Amplifier Design with 30dB DC Gain

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Introduction

Amplifiers abound in the devices we use in our day to day life, such as stereos, loud speakers and cellphones[1]. The purpose of an amplifier is to increase the power in a signal without distorting it. This process is called amplification. For example, amplifiers are used to increase the power in the signal from a microphone so that it can drive a loud speaker[2]. There are many kinds of amplifiers we are now using in circuits design, such as wideband amplifiers, RF amplifiers and so on. These kinds of amplifers hold different functions because of their distinct configurations and parameter settings.

In this case, our purpose is to amplifier a small signal with an magnification of 30 in decibel.

Design Concept

Stage Design

In this project, we are going to design the amplifier with DC gain as 30dB, which is about 31.62 in standard unit. We will need to reach this target by applying common source, common drain and common gate configurations. For these three fundamental amplifiers, the common source configuration is the best suited for realizing the bulk of the gain required design; the common gate configuration has a low input resistance, which makes it only useful in some specific applications such as RF circuits; the common drain (source follower) configration works as a voltage buffer for connecting a high-resistance source to a low-resistance load, its purpose is to equip the

amplifier with a low output resistance[3].

In this project, we will apply the common source configuration to meet the high gain requirement and the common drain configuration as a buffer stage since the output impedence of the common source stage is too high while the load resistance is very low. For each stage, there will be a capacitor to isolate the DC voltage. Figure (1) shows the basic structure of the circuit.

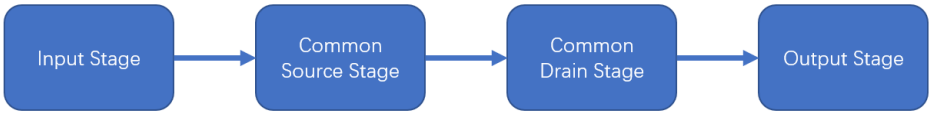

Figure 1: Stage Design of the Circuit

Parameters Extraction of the Transistor

To design the stages of the circuit, firstly we will need to find out the parameters of the transistor such as μ_n, C_{ox} and V_{th}. To get these parameters, we test the performance of the transistor under different conditions and extract these parameters by applying the current expression as in Eq (1).

$$I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{1}$$

The test circuit is shown in Figure (2).

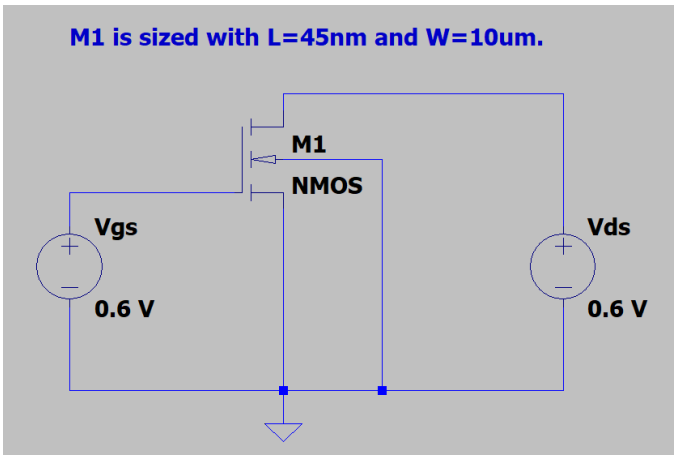

Figure 2: Test Circuit

Then we have the characteristic curves of the transistor. Figure (3) shows the $I_d - V_{gs}$ relation under different V_{DS} conditions ranges from 0.1V to 0.8V. And we can find that the threshold voltage of the transistor is about V_{th}≈0.42V.

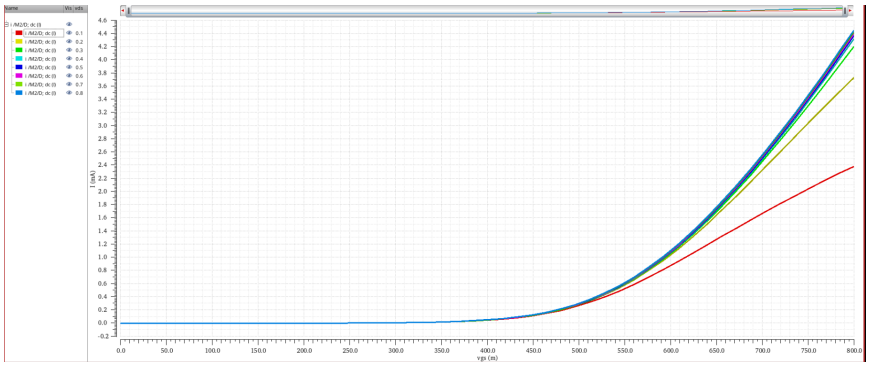

Figure 3: $I_d - V_{gs}$ Relation with Variant V_{DS}

Figure (4) shows the $I_d - V_{DS}$ relation with V_{gs} ranges from 0.1V to 0.8V. The channel length modulation constant is about λ≈0.055V^{-1} by Eq (2). From Eq (1), the value of the carrier constant is about $k^{'} = \mu_n C_{ox}$≈0.483mA/V^2.

$$\frac{1}{r_o} = \frac{\partial I_d}{\partial V_{DS}} = \lambda I_d \tag{2}$$

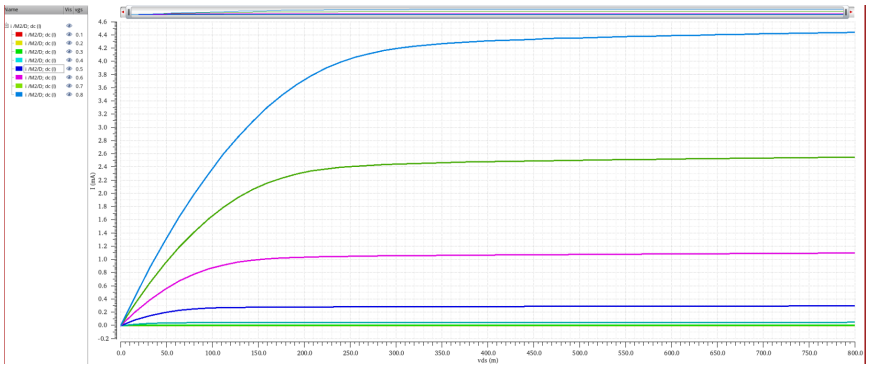

Figure 4: $I_d - V_{DS}$ Relation with variant V_{gs}

In this figure, the channel length modulation resistance is only about $r_o \approx 3600\Omega$, which is small value. To get a high gain of a common source configuration, $r_o = 3600\Omega$ is not enough, a method to enlarge this value is needed. Since the value of r_o is given by Eq (2). To increase the value of r_o, one way is to decrease the value of I_d, the other one is to decrease λ. Both of

them depend on the structure of the transistor, say the value of the channel length L and width W.

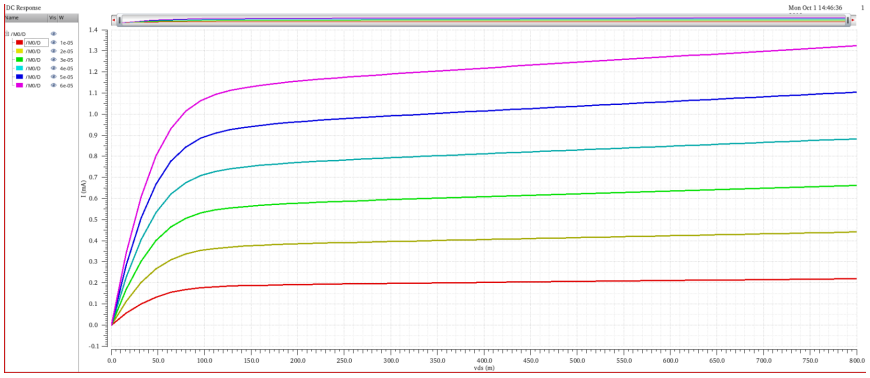

Figure 5: $I_d - V_{DS}$ Relation with Variant W, L=100nm

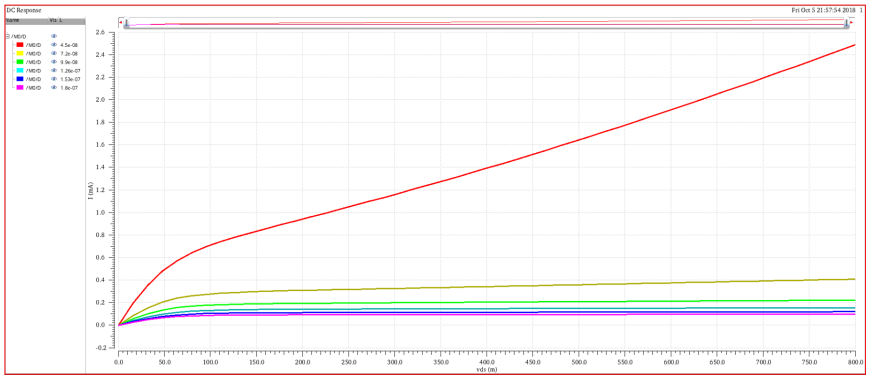

Figure 6: $I_d - V_{DS}$ Relation with Variant L, W=10μm

After trying different channel length and width, Figure (5) shows the $I_d - V_{DS}$ curve with different channel width W ranges from 10μm to 60μm with the channel length as 100nm, and Figure (6) shows the $I_d - V_{DS}$ curve with different channel length L ranges from 45nm to 180nm with the channel widthh as 10μm. In both cases, the value of V_{gs} and V_{ds} are set as 0.5V. The value of r_o is shown in Table (1) and Table (2). The value of r_o is proportional to $\frac{1}{W}$ since the value of $r_o = \frac{2}{\lambda \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2}$. However, the value of r_o increase greatly as the value of L increases not only because L term is proportional to r_o, but also it will effect the CLM constant λ. To ensure that the value of r_o will not effect the amplification in the common soource stage, the value of r_o should be greater than 100kΩ, since in most cases the value of R_D is about several kΩs, we decide to use the transistor with L=180nm which will lead to a greater r_o.

Table 1: r_o with Different W

W **(μm)**	$r_o(\Omega)$
10	22.53k
20	11.42k
30	7.61k
40	5.63k
50	4.55k
60	3.78k

Table 2: r_o with Different L

L **(nm)**	$r_o(\Omega)$
45	0.42k
72	6.02k
99	22.18k
126	46.15k
153	76.59k
180	118.48k

For transistors will channel length L=180nm, its performance parameters are shown in Table (3).

Table 3: Parameter Extration of L=180nm, W=30μm Transistor

V_{th} **(V)**	$\mu_n C_{ox}$ **(mA/V^2)**	λ **(V^{-1})**
0.392	0.285	0.086

Common Source Configuration Design

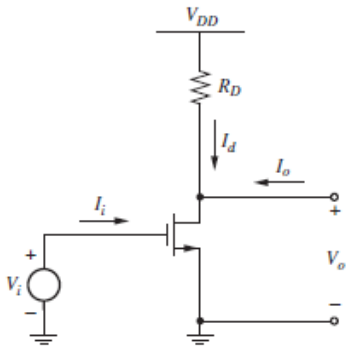

Figure 7: Common Source Configuration

The common source configuration is shown in Figure 7. The amplification coefficient is defined as Eq (3), where g_m is expressed in Eq (4).

$$\|A_v\| = G_m R_{out} = g_m(r_o//R_D) \approx g_m R_D \tag{3}$$

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})(1 + \lambda V_{DS}) = \frac{2I_D}{V_{GS} - V_{th}} \tag{4}$$

According to Kirchhoff Voltage Law,

$$V_{DS} = V_{DD} - I_d R_D \tag{5}$$

Substitute Eq (4) and Eq(5) to Eq (3),

$$\|A_v\| = \frac{2I_D}{V_{GS} - V_{th}} \times \frac{V_{DD} - V_{DS}}{I_D} = \frac{2(V_{DD} - V_{DS})}{V_{GS} - V_{th}} \tag{6}$$

To increase the gain, V_{DS} should be decreased as much as possible and V_{GS} should be close to the threshold voltage V_{th}. In this case, the value we choose is as in Table (4).

Table 4: Parameter Setting in Common Source Configuration

V_{GS} **(mV)**	W **(μm)**	V_{DS} **(mV)**
490	30	200

Then according to Eq (1) and Eq (3),

$$\begin{aligned} I_d &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \\ &= \frac{1}{2} \times 0.285^{-3} \times \frac{30 \times 10^{-6}}{180 \times 10^{-9}}(0.49 - 0.392)^2(1 + 0.086 \times 0.2) \\ &= 232 \times 10^{-6} A \end{aligned}$$

$$R_d = \frac{V_{DD} - V_{DS}}{I_d} = \frac{0.8 - 0.2}{232 \times 10^{-6}} = 2.57k\Omega$$

$$\|A_v\| = \frac{2(V_{DD} - V_{DS})}{V_{GS} - V_{th}} = \frac{2(0.8 - 0.2)}{0.49 - 0.392} \approx 12.24 = 21.76dB$$

Large signal simulation after setting the value of V_{GS}, W and R_D is shown in Large Circuit Section with Figure (13). Figure (8) is the AC voltage gain simulation result.

Figure 8: AC Gain Simulation Result of CS Stage

Table 5: Hand-Calculation vs Simulation Result in CS Stage

	V_{GS} **(mV)**	V_{DS} **(mV)**	I_d **(A)**	A_v **(dB)**
Hand-Calculation	490	200	232×10^{-6}	21.76
Simulation	488	203	232.2×10^{-6}	18.73

Table (5) shows the hand-calculation result and the simulation result.

For large signal analysis, the result in hand-calculation is almost the same with the simulation result while for the AC gain, they are different slightly, which is about 3dB.

There are many reasons that could lead to this result.

1. The exsitance of r_o. The value of r_o in this case is about 38kΩ, which will lead to a decrease about 0.57dB.
2. The carrier mobility μ_n may fluctuate slightly due to the different current flow.

Since the AC gain is about 18.5dB, so we will need two common source stages to realize the 30dB gain requirement.

Common Drain Configuration Design

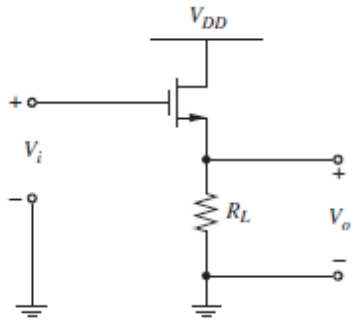

Figure 9: Common Drain Configuration

The common source configuration is shown in Figure 9. The amplification coefficient is defined as Eq (8), where g_m is expressed in Eq (4).

$$A_v = G_m R_{out} = \frac{g_m R_S}{1 + g_m R_S}\left(\frac{1}{g_m} // \frac{1}{g_{mb}} // r_o // R_S\right) \tag{7}$$

The output voltage on the load will be

$$A_{vload} = Av \times \frac{R_{load}}{R_{out} + R_{load}} \tag{8}$$

To make this stage as a perfect buffer stage, the output resistance should as small as possible and enlarge the value of g_m. The expression of g_m is given in Eq (4), which is proportional to $\frac{W}{L}$. Meanwhile, the value of r_o also have a great effect on the value R_{out}, and the value of r_o decrease greatly as $\frac{W}{L}$ increases. So in this case we choose a large W as 80μm and a small channel length as $L = 45$nm. And of course to enlarge g_m, the value of V_{GS} is also set as a large value. Table (6)

Table 6: Parameter Setting in Common Drain Configuration

V_{GS} **(mV)**	W **(μm)**	L **(nm)**	R_S Ω
680	80	45	125

Then according to Eq (1) and Eq (4),

$$\begin{aligned} I_d &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2(1+\lambda V_{DS}) \\ &\approx \frac{1}{2}\times 0.285^{-3}\times\frac{80\times10^{-6}}{45\times10^{-9}}(0.68-0.392)^2 \\ &= 2.10\times10^{-3}A \end{aligned}$$

$$\begin{aligned} g_m &= \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})(1+\lambda V_{DS}) \\ &\approx 0.285^{-3}\times\frac{80\times10^{-6}}{45\times10^{-9}}(0.68-0.392) \\ &= 0.0146A/V \end{aligned}$$

$$V_{DS} = V_{DD} - I_{DS}R_S = 0.8 - 2.1\times10^{-3}\times125 = 537.5mV$$

Then the output resistance is

$$R_{out} = \frac{1}{g_m}//\frac{1}{g_{mb}}//r_o//R_S \approx 125//68.5 = 44.25\Omega$$

The short-circuit transconductance is

$$G_M = \frac{g_m R_S}{1+g_m R_S} = \frac{0.0146\times125}{1+0.0146\times125} = 0.65$$

Then the common drain amplification is

$$A_{vload} = G_M\frac{R_{load}}{R_{out}+R_{load}} = 0.65\times\frac{50}{44.25+50} = 0.35 = -9.11dB$$

Large signal simulation after setting the value of V_{GS}, W and R_D is shown in Large Circuit Section with Figure (13). Figure (10) is the AC voltage gain simulation result.

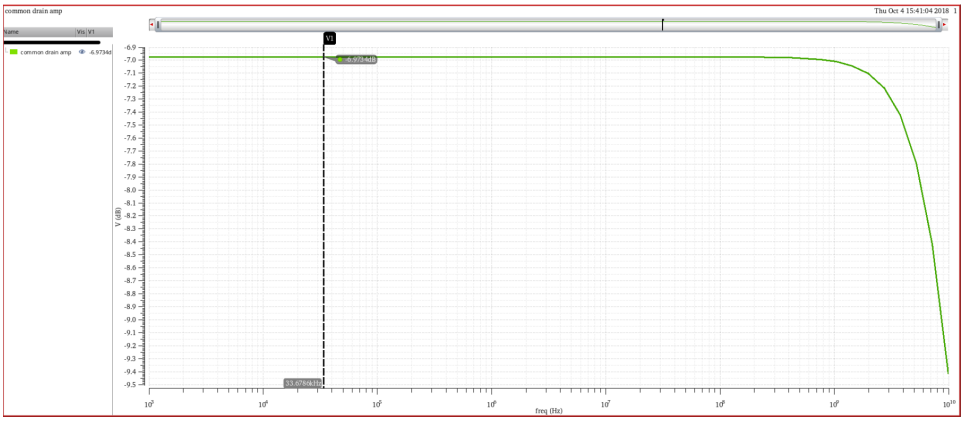

Figure 10: AC Gain Simulation Result of CD Stage

Table 7: Hand-Calculation vs Simulation Result in CD Stage

	V_{GS} **(mV)**	V_{DS} **(mV)**	I_d **(A)**	A_{vload} **(dB)**
Hand-Calculation	680.0	537.5	2.100×10^{-3}	-9.11
Simulation	679.6	543.3	2.085×10^{-3}	-6.97

Table (7) shows the hand-calculation result and the simulation result.

For large signal analysis, the result in hand-calculation is almost the same with the simulation result while for the AC gain, they are different slightly, which is about 2.14dB. The simulation result is much better than the hand-calculation expectation.

There are many reasons that could lead to this result.

1. In hand-calculation, the body effect is ignored which means the actual value of R_{out} is much smaller than the expected one.
2. The channel length modulation of short channel transistor is much different with a long channel one, which means its performance is not as predictable as a normal one.
3. The threshold voltage V_{th} is enlarged because of the body effect, and it will lead to the decrease of g_m.

Complete Circuit

With the designs above, the complete circuit is shown in Figure (11).

To erase the DC effect of the former stage, all stage are isolated with each other by a capacitor with the capacitance of 18nF. However, it will have an effect to the AC circuit since a capacitor will have an impedance as $Z_C = \frac{1}{j\omega C}$[4]. The AC circuit diagram is shown in Figure (12).

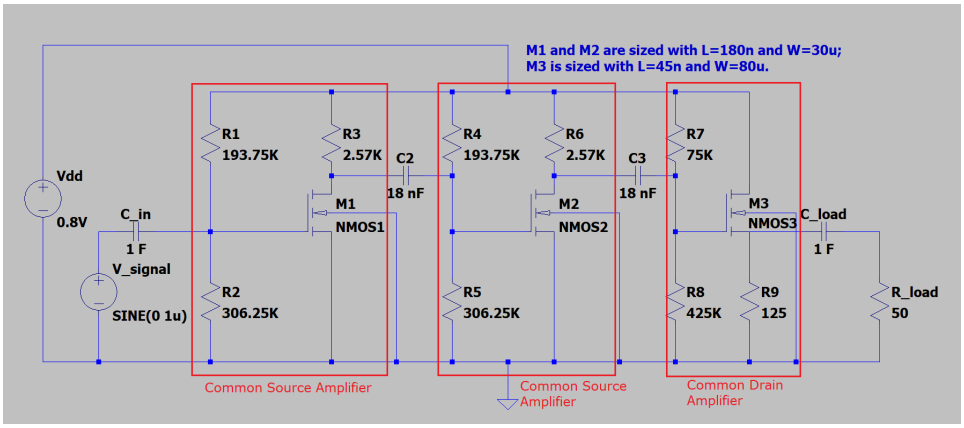

Figure 11: Complete Circuit with Stage Division

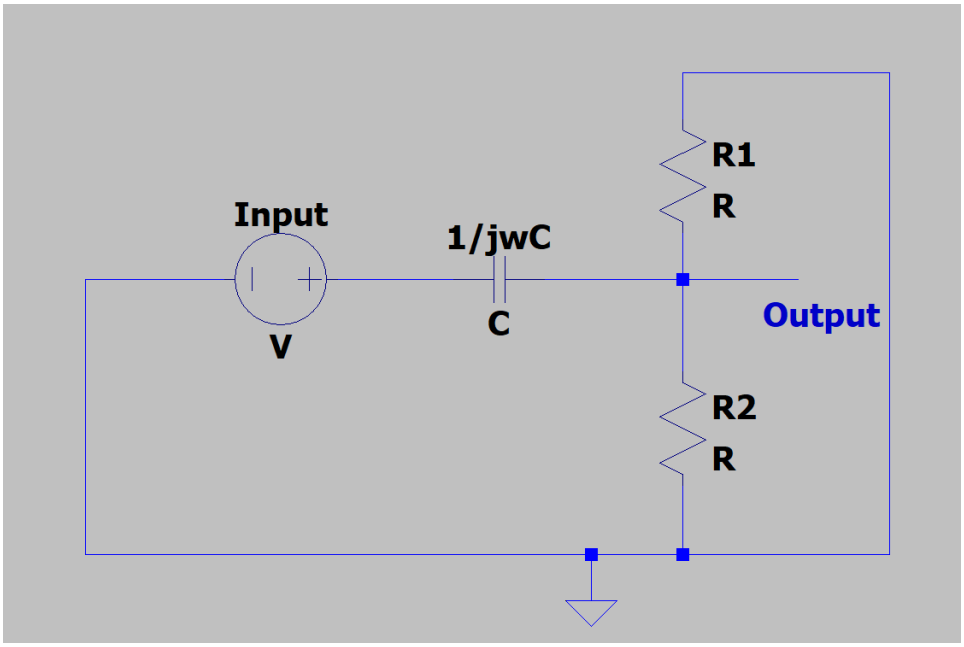

Figure 12: AC Circuit with Capacitor

To erase the AC effect from the capacitor, one way is to increase the value of voltage divider's resistors. It is also for the power consumption consideration since the larger resistance will have less power consumption if the voltage is fixed.

Conclusion

In conclusion, this design contains two identical common source stages and one common drain stage. For each stage, the parameter setting and some of the results are shown in Table (8).

Table 8: Parameter Setting & Some Results

	V_{GS}**(mV)**	$W(\mu$**m)**	L**(nm)**	$R_D/R_S(\Omega)$	V_{DS}**(mV)**	I_d**(A)**
CS	488.2	30	180	2.57k	203	232.2×10^{-6}
CD	679.6	80	45	125	543.3	2.085×10^{-3}

The DC simulation is shown in Figure (13) and the AC gain simulation is shown in Figure (14). The DC gain is about 30.35dB, wich fits the requirement. The power consumption in all is about 824.95μW.

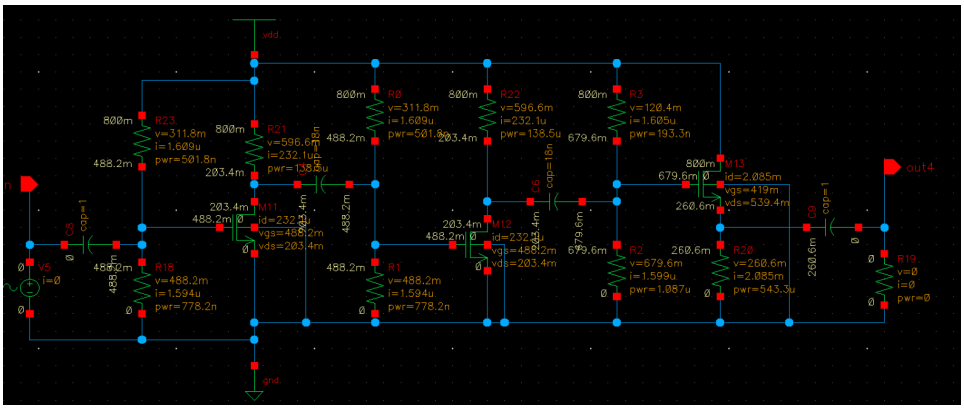

Figure 13: DC Simulation of Complete Circuit

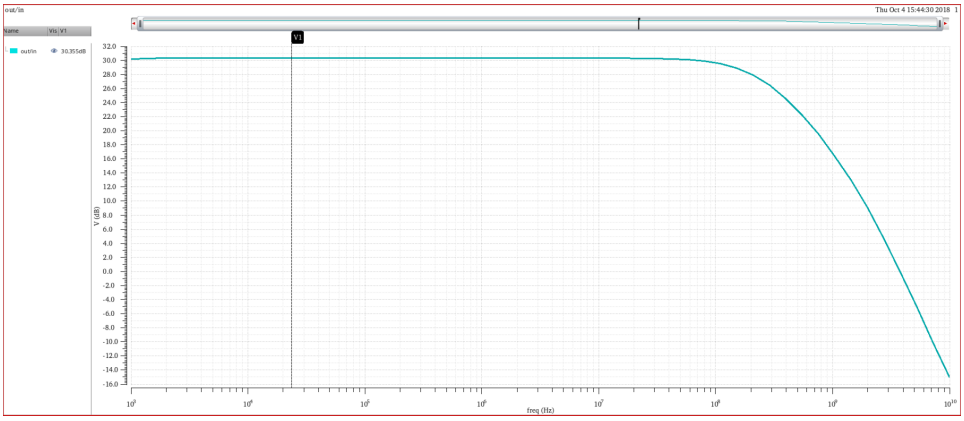

Figure 14: AC Simulation of Complete Circuit

References

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