EE479L Fall 2018 Design Project#2 Report
4-Level Supply Independent Current Mirror

HONGXIANG GAO 8095639536
MINGYANG LI 3349336154
University of Southern California
November 10, 2018

Contents

1 Introduction

The operational amplifier ("op amp") is the most versatile and widely used type of analog IC, used in audio and voltage amplifiers, signal conditioners, signal converters, oscillators, and analog computing systems. Almost every electronic device uses at least one op amp.[1]

An ideal op amp with a single-ended output has a differential input, infinite voltage gain, infinite input resistance, and zero output resistance.A conceptual schematic diagram is shown in Figure 1. While actual op amps do not have these ideal characteristics, their performance is usually sufficiently good that the circuit behavior closely approximates that of an ideal op amp in most applications.

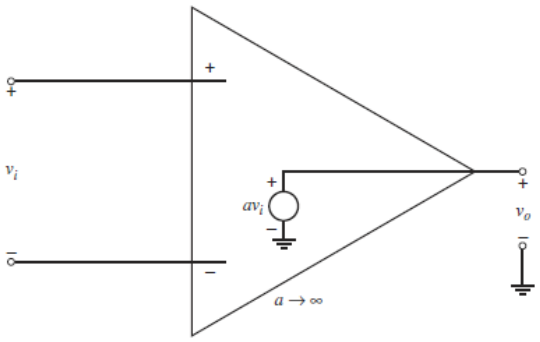

Figure 1: Ideal operational amplifier

In op-amp design, bipolar transistors offer many advantages over their CMOS counterparts, such as higher transconductance for a given current, higher gain, higher speed, lower input-referred offset voltage and lower input-referred noise voltage. However, CMOS technologies have become dominant in building the digital portions of signal-processing systems because CMOS digital circuits are smaller and dissipate less power than their bipolar counterparts. To reduce system cost and increase portability, analog and digital circuits are now often integrated together, providing a strong economic incentive to use CMOS op amps.[2]

In building a CMOS operational amplifier, to support the current biasing, a supply-independent current biasing startup circuit is needed.[3] A basic configuration is shown in Figure 2. In this configuration, the current in the output branch is[4]

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_S^2}(1 - \frac{1}{\sqrt{K}})^2$$

To improve the performance of this design, such as output swing, output

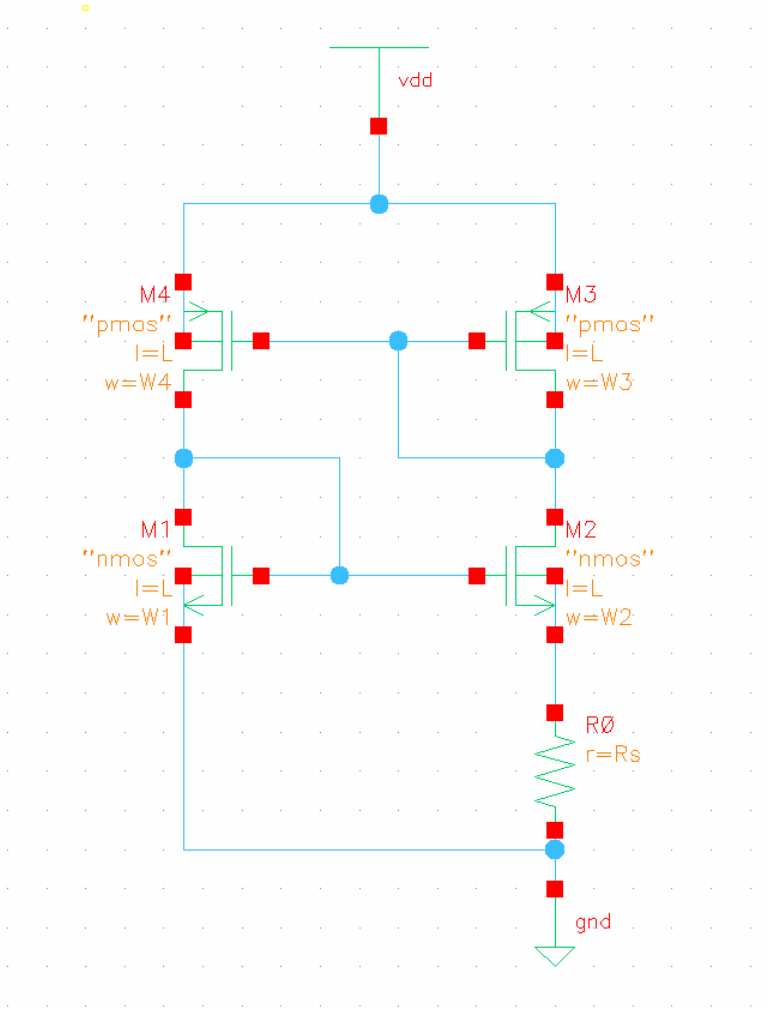

Figure 2: Basic Configuration of Supply-Independent Current Mirror

resistance and power supply sensitivity, a better configuration is designed as in Figure 3. The new design has a much better performance compared with the basic one.

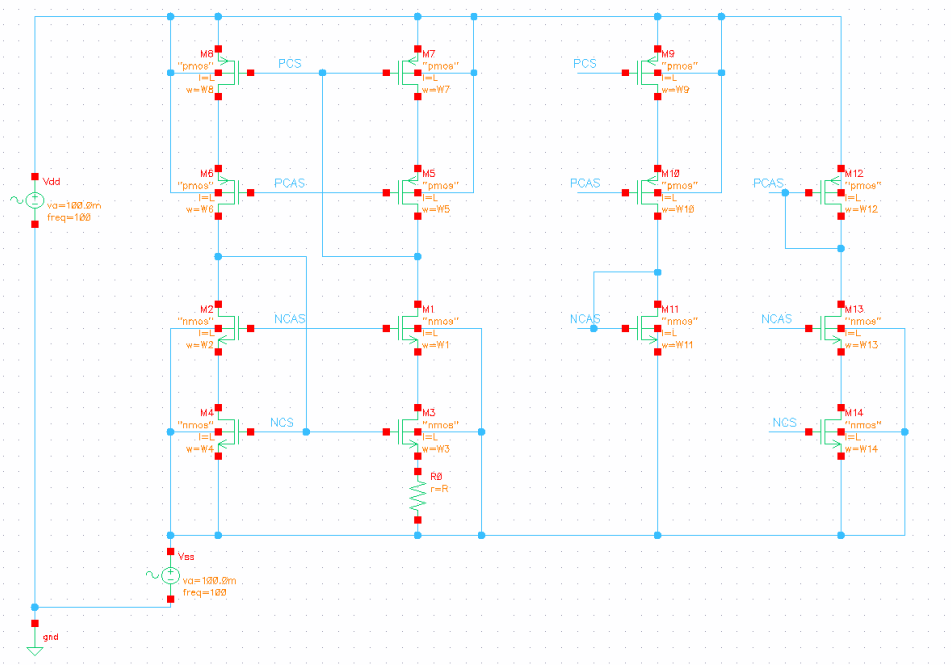

Figure 3: Configuration of 4-Level Supply-Independent Current Mirror

2 Design Concept

In this design project, we will apply the strategy called "Divide and Conquer", or say superposition in the other word. That is, build the circuit step by step and make sure each of them are working perfectly and then add them up to a complete one.

2.1 Parameter of MOSFETS

Firstly, we will need to find out the parameters of the NMOS and the PMOS such as μC_{ox}, V_{th} and λ so that we can do hand calculation to find out the approximate designing value. Since the channel length modulation will effect these parameters, so we choose a decent value of the channel length as 180nm, which is also one of the standard fabrication processes being used nowadays.

We applied the test circuit as Figure 4 to measure the properties of the MOSFETs (It is also used for NMOS testing). Table 1 shows the hand calculation result of V_{th}, μC_{ox} and λ of both NMOS and PMOS with $W = 30\mu m$ and $L = 180nm$.

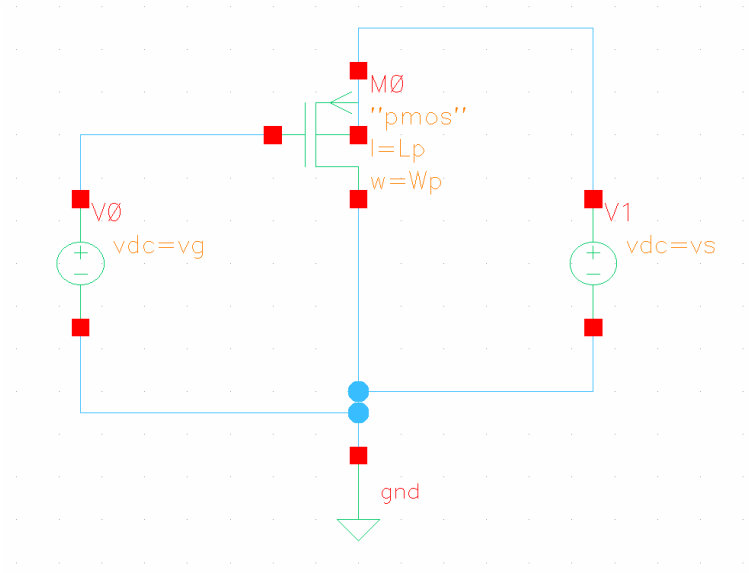

Figure 4: Parameter Test Circuit

Table 1: Parameter Extration of L=180nm, W=30μm Transistor

	V_{th} **(V)**	μC_{ox} **(mA/V^2)**	λ **(V^{-1})**
NMOS	0.392	0.385	0.086
PMOS	-0.325	0.0334	-0.027

2.2 Voltage Setting

For simplicity, we set the V_{DD} as 1V and V_{SS} as 0V. Then the 10% voltage fluctuation would be about 100mV.

For V_{NCS}, which is decided by M4, its value is

$$V_{NCS} = V_{th,n} + V_{dsat4} \tag{1}$$

We take the value of V_{dsat4} as 50mV, which is a proper value to keep M4 is always in saturation mode even there is voltage fluctuation. Then the value of V_{NCS} is about 442mV. Similarly, to ensure M7 is in saturation region, the value of V_{PCS} is

$$V_{PCS} = V_{DD} - |V_{th,p}| - |V_{dsat7}| \tag{2}$$

Setting the value of $|V_{dsat7}|$ as 50mV, the value of V_{PCS} is about 625mV.

To make sure that M2 is in saturation mode, we have

$$\begin{aligned} V_{NCS} &> V_{NCAS} - V_{th,n} \\ \Rightarrow V_{NCAS} &< V_{NCS} + V_{th,n} \end{aligned} \tag{3}$$

Similarly, to make sure M5 is in saturation, we have

$$\begin{aligned} V_{source,5} - V_{PCS} &> V_{source,5} - V_{PCAS} - |V_{th,p}| \\ \Rightarrow V_{PCAS} &> V_{PCS} - |V_{th,p}| \end{aligned} \tag{4}$$

For M6 and M1, we have

$$\begin{aligned} V_{source,6} - V_{NCS} &> V_{source,6} - V_{PCAS} - |V_{th,p}| \\ V_{PCS} - V_{source,1} &> V_{NCAS} - V_{source,1} - V_{th,n} \\ \Rightarrow V_{PCAS} &> V_{NCS} - |V_{th,p}| \\ \Rightarrow V_{NCAS} &< V_{PCS} + V_{th,n} \end{aligned} \tag{5}$$

For the right two branches, for M10 and M13, we have

$$\begin{aligned} V_{source,10} - V_{NCAS} &> V_{source,10} - V_{PCAS} - |V_{th,p}| \\ V_{PCAS} - V_{source,1} &> V_{NCAS} - V_{drain,1} - V_{th,n} \\ \Rightarrow V_{NCAS} &< V_{PCAS} + |V_{th,p}| \\ \Rightarrow V_{NCAS} &< V_{PCAS} + V_{th,n} \end{aligned} \tag{6}$$

With Equation 1, 2, 3, 4, 5, 6, we can conclude the constraints of V_{NCS}, V_{PCS}, V_{NCAS} and V_{PCAS} as:

$$\begin{aligned} V_{NCS} &= V_{th,n} + V_{dsat4} = 442mV \\ V_{PCS} &= V_{DD} - |V_{th,p}| - |V_{dsat7}| = 625mV \\ V_{NCAS} &< V_{NCS} + V_{th,n} \Rightarrow V_{NCAS} < 834mV \\ V_{PCAS} &> V_{PCS} - |V_{th,p}| \Rightarrow V_{PCAS} > 300mV \\ V_{NCAS} - V_{PCAS} &< |V_{th,p}| = 325mV \end{aligned} \tag{7}$$

Then we choose the value of V_{NCS}, V_{PCS}, V_{NCAS} and V_{PCAS} as:

$$\begin{aligned} V_{NCS} &= 442mV \\ V_{PCS} &= 625mV \\ V_{NCAS} &= 640mV \\ V_{PCAS} &= 380mV \end{aligned} \tag{8}$$

2.3 Bottom Part of Current Mirror

For divide and conquer strategy, we choose the bottom part as the first section to handle with, since it is the core part to decide the current going through the current mirror.

Firstly, we will decide the size of M4, since we have known the $V_{gate,4}$ and $V_{source,4}$, and we have assumed that $V_{dsat,4}$ is around 50mV, then we can decide the size of M4. Assume the value of $V_{DS,4}$ is around 235mV to ensure M4 is in saturation mode. We have the current through M4 as:

$$\begin{aligned} I_4 &= \frac{1}{2}\mu_n C_{ox}\frac{W_4}{L_4}V_{dsat,4}^2(1+\lambda V_{DS}) \\ 25\times10^{-6} &= \frac{1}{2}\times 3.85\times10^{-4}\times\frac{W_4}{L_4}\times(50\times10^{-3})^2\times(1+0.086\cdot0.235) \\ \Rightarrow \quad \frac{W_4}{L_4} &\approx 40 \\ \Rightarrow \quad W_4 &\approx 7.2\mu m \end{aligned} \tag{9}$$

The simulation result is as Figure 5. The current I_4 is 24.96μA, which is close to 25μA.

For M3, we have the current relation as:

$$I_{out} = \frac{2}{\mu_n C_{ox}\frac{W_4}{L_4}}\cdot\frac{1}{R^2}(1-\sqrt{\frac{W_4}{L_4}/\frac{W_3}{L_3}})^2 \tag{10}$$

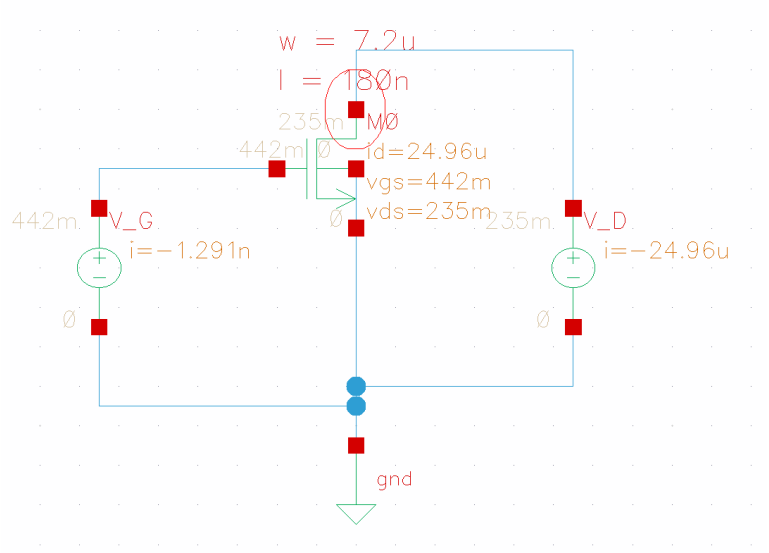

Figure 5: Simulation of M4

If we take R as 1500Ω, Then we have

$$\begin{aligned} & \frac{W_3}{L_3} \approx 100 \\ \Rightarrow \quad & W_3 \approx 18\mu m \end{aligned} \tag{11}$$

To ensure that M3 is in saturation mode, we set the value of $V_{DS,3}$ as 155mV. The simulation result is as Figure 6. The current go through M3 is exactly 25μA.

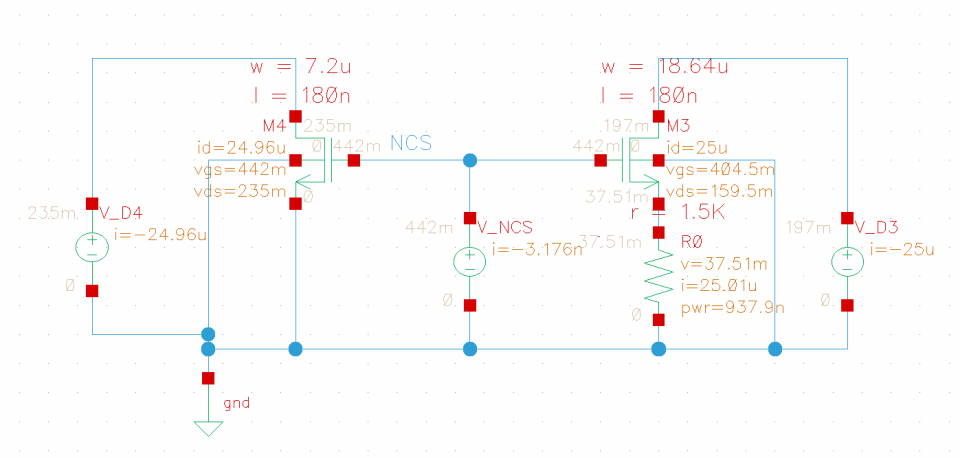

Figure 6: Simulation of M3 and M4

For M1 and M2, there purposes are to keep both M3 and M4 in saturation mode. And in previous assumptions, we have

$$\begin{aligned} V_{gate,1} = V_{NCAS} &= 640mV, \\ V_{source,1} &= 235mV, \\ V_{drain,1} = V_{NCS} &= 442mV, \\ V_{gate,2} = V_{NCAS} &= 640mV, \\ V_{source,2} &= 197.5mV, \\ V_{drain,2} = V_{PCAS} &= 380mV \end{aligned} \tag{12}$$

With the Equation of saturation current as

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{13}$$

We can calculate the value of $\frac{W_1}{L_1}$ and $\frac{W_2}{L_2}$ as

$$\begin{aligned} \frac{W_1}{L_1} &\approx 111 \Rightarrow W_1 = 20\mu m \\ \frac{W_2}{L_2} &\approx 333 \Rightarrow W_2 = 60\mu m \end{aligned} \tag{14}$$

The simulation result is shown as Figure 7. All the transistors are in saturation mode.

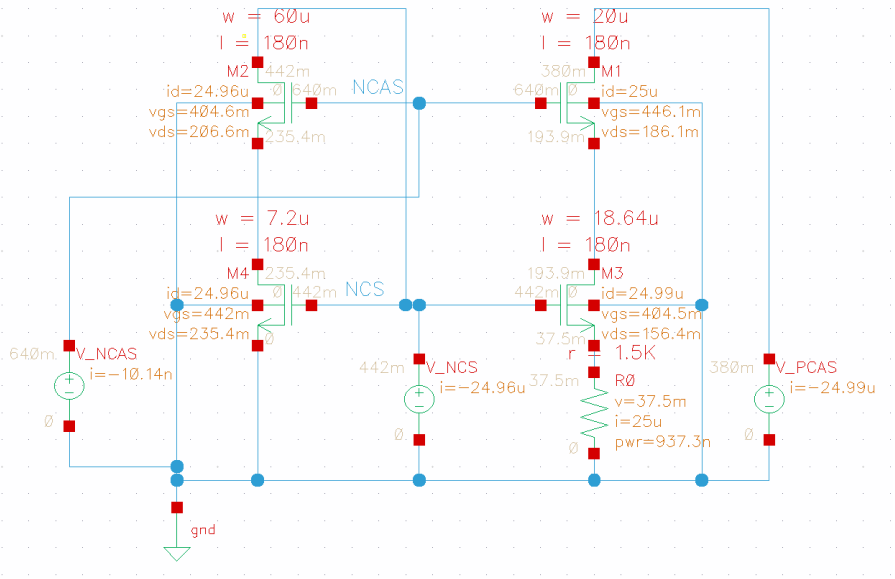

Figure 7: Simulation of Bottom Part of Current Mirror

2.4 Upper Part of Current Mirror

For the PMOS part, it is much more easy to handle since there is no resistance in the circuit. Firstly, we can handle M7 and M8. We set the value of $V_{drain,7}$ and $V_{drain,8}$ as 890mV and 825mV to make sure both of them are in saturation mode. In conclusion, we have:

$$\begin{aligned} V_{gate,7} &= V_{PCS} = 625mV, \\ V_{source,7} &= V_{DD} = 1V, \\ V_{drain,7} &= 890mV, \\ V_{gate,8} &= V_{PCS} = 625mV, \\ V_{source,8} &= V_{DD} = 1V, \\ V_{drain,8} &= 825mV \end{aligned} \tag{15}$$

With Equation 13, we can calculate the value of $\frac{W_7}{L_7}$ and $\frac{W_8}{L_8}$ as

$$\begin{aligned} \frac{W_7}{L_7} &\approx 850 \Rightarrow W_7 = 153\mu m \\ \frac{W_8}{L_8} &\approx 820 \Rightarrow W_8 = 147.6\mu m \end{aligned} \tag{16}$$

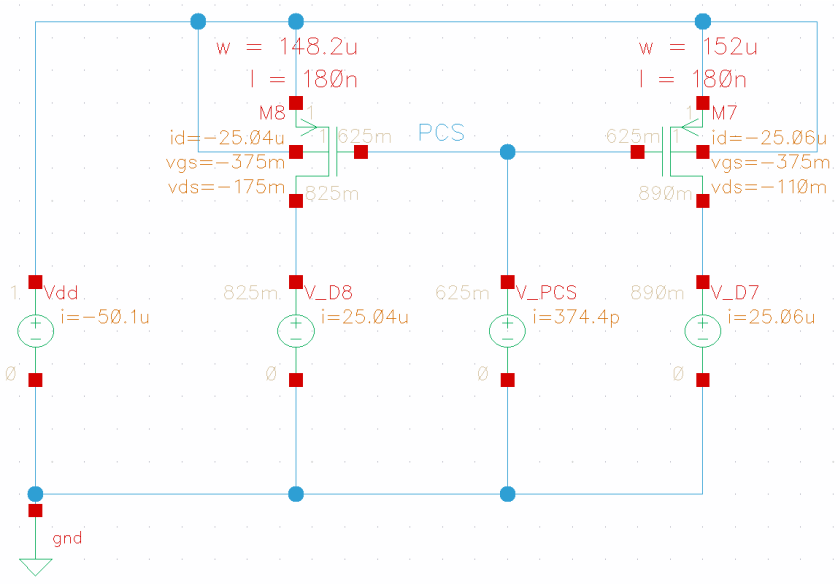

Figure 8: Simulation of M7 and M8

Figure 8 shows the simulation result and both of them are in saturation mode. Similarly, the purposes of M5 and M6 are to keep M7 and M8 in saturation mode, we have:

$$
\begin{aligned}
V_{gate,5} = V_{PACS} &= 380mV, \\
V_{source,5} &= 890mV, \\
V_{drain,5} = V_{PCS} &= 625mV, \\
V_{gate,6} = V_{PCAS} &= 380mV, \\
V_{source,6} &= 825mV, \\
V_{drain,6} = V_{NCS} &= 442mV
\end{aligned} \tag{17}
$$

With Equation 13, we can calculate the value of $\frac{W_7}{L_7}$ and $\frac{W_8}{L_8}$ as

$$
\begin{aligned}
\frac{W_5}{L_5} &\approx 111 \Rightarrow W_5 = 20\mu m \\
\frac{W_6}{L_6} &\approx 445 \Rightarrow W_6 = 80\mu m
\end{aligned} \tag{18}
$$

Figure 9 shows the simulation result and all the transistors are in saturation mode.

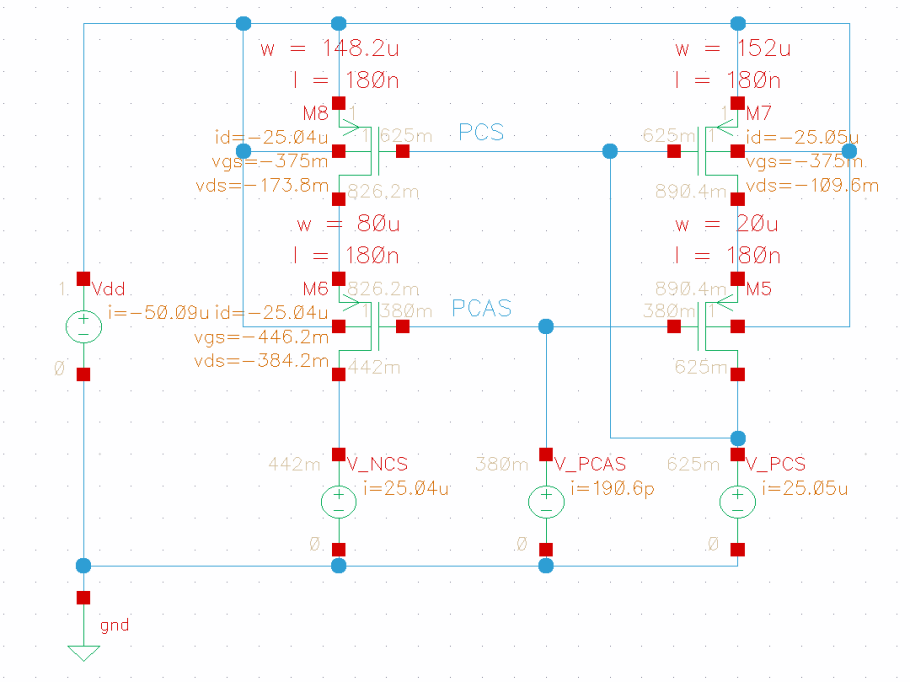

Figure 9: Simulation of Upper Part of Current Mirror

2.5 Current Mirror

After we have add them together, Figure 10 shows the simulation result of the complete current mirror. The current go through both of the two branches are very close to 25μA.

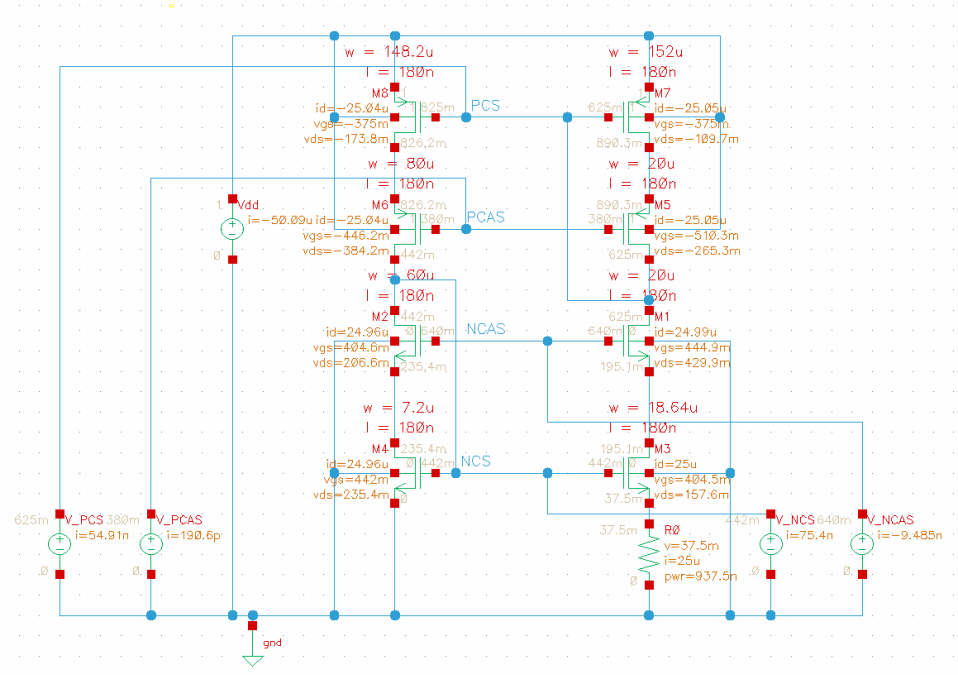

Figure 10: Simulation of Compelete Current Mirror

2.6 Bias & Feedback Generation Circuit

The right two branches are for biasing the voltage of V_{NCAS} and V_{PCAS}. For the left branch, M11 is for biasing the value of V_{NCAS}, and the other two, say M9 and M10 are for feedback of V_{PCS} and V_{PCAS}. Similarly, for the right branch, M12 is for biasing the value of V_{PCAS}, and M13 and M14 are for feedback of V_{NCAS} and V_{NCS}.

For M11 and M12, with the value of V_{NCAS} and V_{PCAS} decided as 640mV and 380mV, we can calculate the value of $\frac{W_{11}}{L_{11}}$ and $\frac{W_{12}}{L_{12}}$ with equation 13.

$$\begin{aligned} \frac{W_{11}}{L_{11}} &\approx 2.67 \Rightarrow W_{11} = 480nm \\ \frac{W_{12}}{L_{12}} &\approx 21.5 \Rightarrow W_{12} = 3.87\mu m \end{aligned} \tag{19}$$

For M9, M10, M13, M14, assume that $V_{drain,9} = V_{source,10}$=900mV and $V_{source,13} = V_{drain,14}$=160mV, then we have:

$$\begin{aligned} V_{gate,9} = 625mV,\ \ V_{source,9} = 1V,\ \ V_{drain,9} = 900mV, \\ V_{gate,10} = 380mV,\ \ V_{source,10} = 900mV,\ \ V_{drain,10} = 640mV, \\ V_{gate,13} = 640mV,\ \ V_{source,13} = 160mV,\ \ V_{drain,13} = 380mV, \\ V_{gate,14} = 442mV,\ \ V_{source,14} = 0V,\ \ V_{drain,14} = 160mV \end{aligned} \tag{20}$$

With hand calculation, we have:

$$\begin{aligned} \frac{W_9}{L_9} \approx 850 \Rightarrow W_9 = 153\mu m, \quad \frac{W_{10}}{L_{10}} \approx 111 \Rightarrow W_{10} = 20\mu m \\ \frac{W_{13}}{L_{13}} \approx 55 \Rightarrow W_{13} = 10\mu m, \quad \frac{W_{14}}{L_{14}} \approx 40 \Rightarrow W_{14} = 7.2\mu m \end{aligned} \tag{21}$$

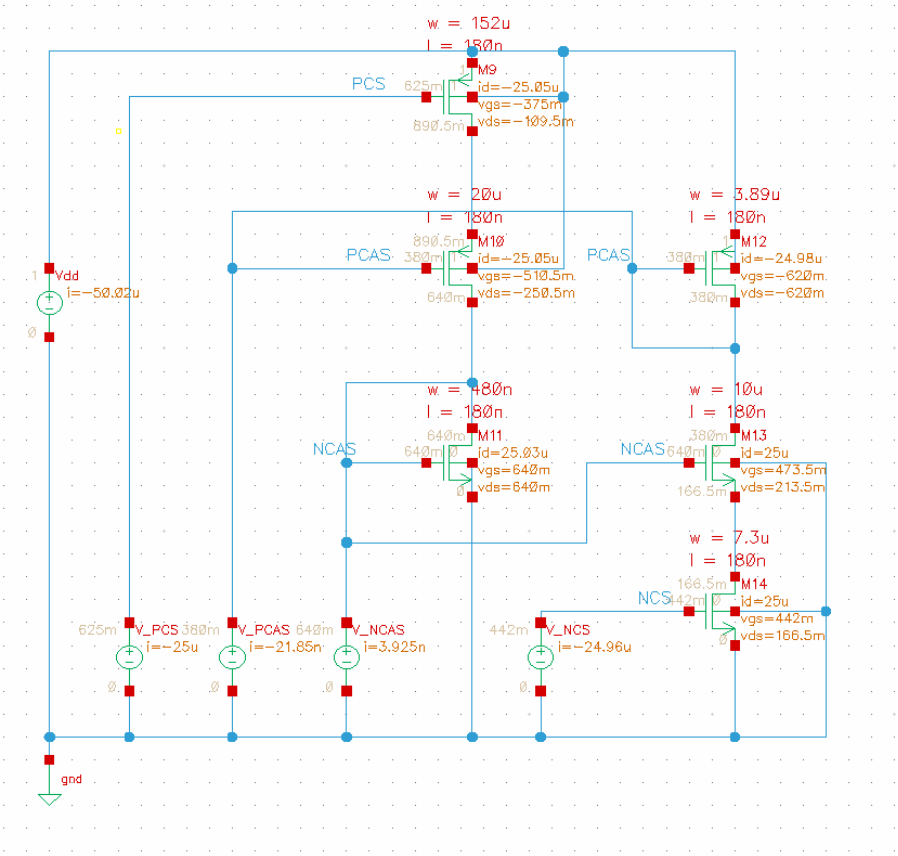

Figure 11: Simulation of Bias Circuit

After some adjustment, the simulation result is shown in Figure 11. For each biasing branch, we designed the sizing of the transistors so that the current go through each branch is very close to 25μA, which will have a better feedback performance in stabling the biasing voltage in the current mirror, and all the transistors are in saturation mode.

3 Conclusion & Simulation Result

3.1 Simulation Result

In conclusion, we have designed a 4-level supply independent current mirror with designed dc biasing current as 25μA as shown in Figure 12.

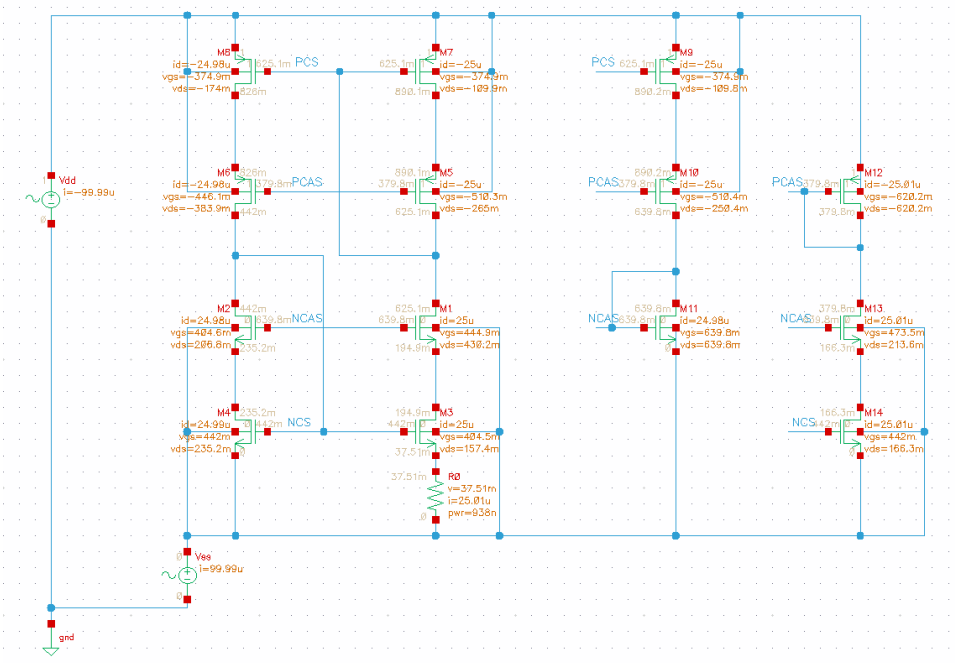

Figure 12: Simulation of Complete Circuit

To ensure each of the transistor are in saturation mode, we need to designed the biasing voltage of circuit, say V_{NCS}, V_{NCAS}, V_{PCS} and V_{PCAS}. Table 3 shows the differenc of biasing voltage between hand calculation and simulation result.

Table 2: Biasing Voltage: Hand Calculation vs Simulation

	V_{NCS} **(mV)**	V_{NCAS} **(mV)**	V_{PCS} **(mV)**	V_{PCAS} **(mV)**
Hand Calculation	442	640	625	380
Simulation	442	639.8	625.1	379.8

The sizing and voltage of each transistor are shown in Table 3.

Table 3: Sizing & Voltage: Hand Calculation vs Simulation

	M_1	M_2	M_3	M_4	M_5	M_6	M_7
$\frac{W}{L}$(Hand)	111	333	100	40	111	445	850
$\frac{W}{L}$(Simu)	111	333	103.6	40	111	445	844.4
$W\ (\mu m)$(Hand)	20	60	18	7.2	20	80	153
$W\ (\mu m)$(Simu)	20	60	18.64	7.203	20	80	152
$L\ (nm)$(Hand)	180	180	180	180	180	180	180
$L\ (nm)$(Simu)	180	180	180	180	180	180	180
$V_{gate}\ (mV)$(Hand)	640	640	442	442	380	380	625
$V_{gate}\ (mV)$(Simu)	639.8	639.8	442	442	379.8	379.8	625.1
$V_{source}\ (mV)$(Hand)	197.5	235	37.5	0	890	825	1000
$V_{source}\ (mV)$(Simu)	194.9	235.2	37.51	0	890.1	826	1000
$V_{drain}\ (mV)$(Hand)	625	442	197.5	235	625	442	890
$V_{drain}\ (mV)$(Simu)	625.1	442	194.9	235.2	625.1	442	890.1
	M_8	M_9	M_{10}	M_{11}	M_{12}	M_{13}	M_{14}
$\frac{W}{L}$(Hand)	820	850	111	2.67	21.5	55	40
$\frac{W}{L}$(Simu)	823.3	844.4	111	2.67	21.6	55.6	40.6
$W\ (\mu m)$(Hand)	147.6	153	20	0.48	3.87	9.9	7.2
$W\ (\mu m)$(Simu)	148.2	152	20	0.48	3.89	10	7.3
$L\ (nm)$(Hand)	180	180	180	180	180	180	180
$L\ (nm)$(Simun)	180	180	180	180	180	180	180
$V_{gate}\ (mV)$(Hand)	625	625	380	640	380	640	442
$V_{gate}\ (mV)$(Simu)	625.1	625.1	379.8	639.8	379.8	639.8	442
$V_{source}\ (mV)$(Hand)	1000	1000	890	0	1000	160	0
$V_{source}\ (mV)$(Simu)	1000	1000	890.2	0	1000	166.3	0
$V_{drain}\ (mV)$(Hand)	825	890	640	640	380	380	160
$V_{drain}\ (mV)$(Simu)	826	890.2	639.8	639.8	379.8	379.8	166.3

3.2 Supply Dependency Analysis

Figure 13 shows the simulation result with V_{DD} fluctuate as 10%, the current in the left and right branches will change about 0.018μA and 0.013μA correspondingly.

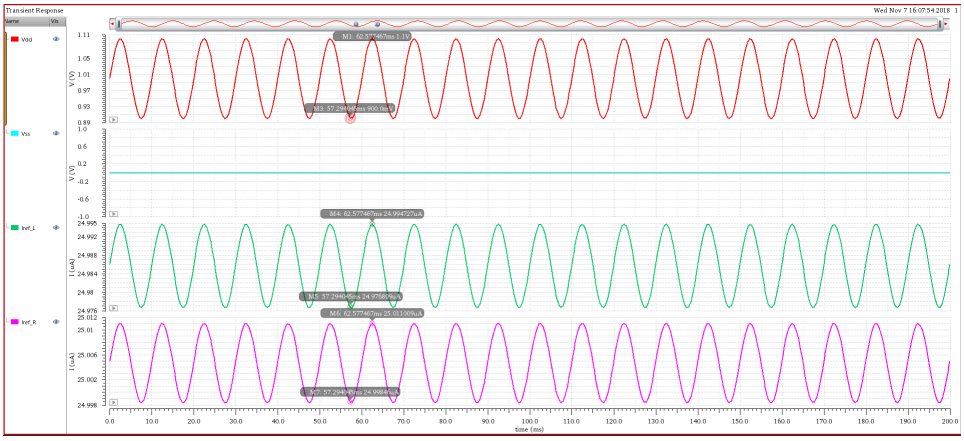

Figure 13: Simulation with V_{DD} Fluctuation

Figure 14 shows the simulation result with V_{SS} fluctuate as 10%, the current in the left and right branches will change about 0.024μA and 0.012μA correspondingly.

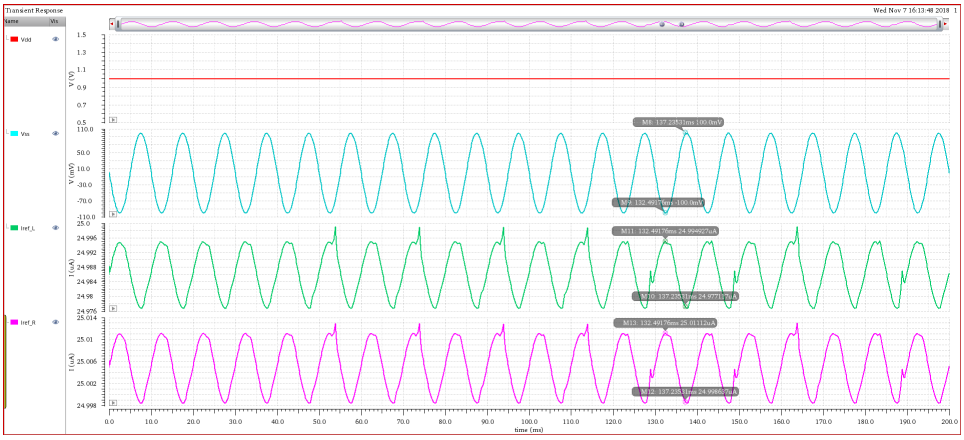

Figure 14: Simulation with V_{SS} Fluctuation

Figure 15 shows the simulation result with V_{DD} and V_{SS} fluctuate as 10% with 180 degree phase difference, the current in the left and right branches will change about 0.031μA and 0.024μA correspondingly.

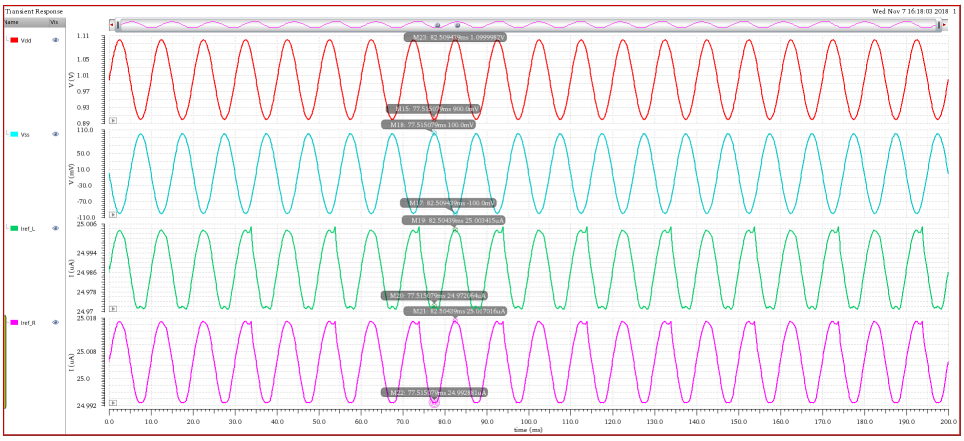

Figure 15: Simulation with V_{DD} and V_{SS} Fluctuation Out of Phase

Figure 16 shows the simulation result with V_{DD} and V_{SS} fluctuate as 10% without phase difference, the current in the left and right branches changes slightly so that we take it as stable one.

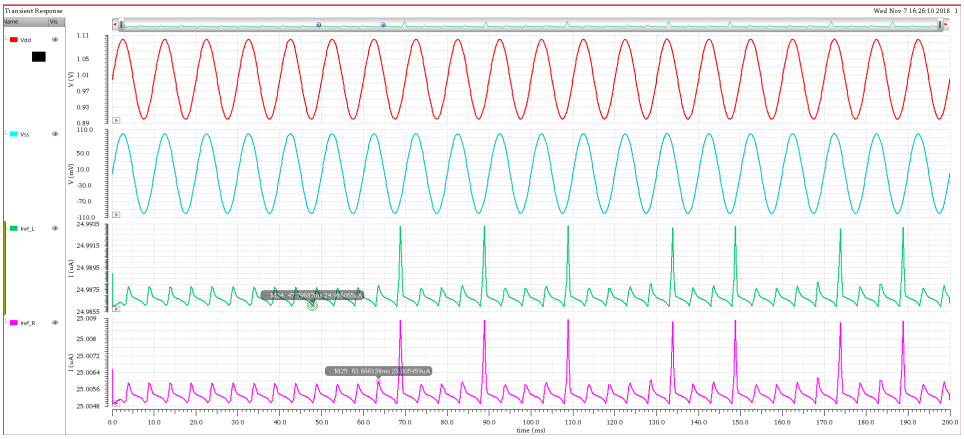

Figure 16: Simulation with V_{DD} and V_{SS} Fluctuation In Phase

In conclusion, Table 4 shows the sensitivity of each case. All the Δ value are taking peak-to-peak value.

Table 4: Sensitivity Analysis

Left Branch	$\Delta I_{ref,L}$ (μA)	$I_{ref,L}$ (μA)	$\frac{\Delta I_{ref,L}}{I_{ref,L}} / \frac{\Delta V}{V}$
V_{DD}	0.018	24.986	3.602×10^{-3}
V_{SS}	0.024	24.983	4.803×10^{-3}
V_{DD} & V_{SS}	0.031	24.988	6.203×10^{-3}
Right Branch	$\Delta I_{ref,R}$ (μA)	$I_{ref,R}$ (μA)	$\frac{\Delta I_{ref,R}}{I_{ref,R}} / \frac{\Delta V}{V}$
V_{DD}	0.013	25.005	2.599×10^{-3}
V_{SS}	0.012	25.005	2.399×10^{-3}
V_{DD} & V_{SS}	0.024	25.005	4.799×10^{-3}

From Table 4, we can see that for V_{DD} fluctuation, the output reference current keep the shape of a sinusoidal curve, while for V_{SS} changing, it will have some spikes at the peak points. It is because that our resistance R is directly connected to the ground, and the value of V_{SS} will have a more direct influence on the current. And we can find that the current in the right branch is more stable than the left one, so we can using the right branch to achieve the stable current biasing.

References

1. B. Carter. *Op Amps for Everyone*. Elsevier Science, 2003.

2. Paul R Gray, Paul Hurst, Robert G Meyer, and Stephen Lewis. *Analysis and design of analog integrated circuits*. Wiley, 2001.

3. A. Boni. Op-amps and startup circuits for cmos bandgap references with near 1-v supply. *IEEE Journal of Solid-State Circuits*, 37(10):1339–1343, Oct 2002.

4. B. Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill series in electrical and computer engineering. McGraw-Hill, 2001.