EE479L Fall 2018 Design Project#3 Report
Folded Cascode Operational Amplifier

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Contents

1 Introduction

The operational amplifier ("op amp") is the most versatile and widely used type of analog IC, used in audio and voltage amplifiers, signal conditioners, signal converters, oscillators, and analog computing systems. Almost every electronic device uses at least one op amp.[1]

An ideal op amp with a single-ended output has a differential input, infinite voltage gain, infinite input resistance, and zero output resistance.A conceptual schematic diagram is shown in Figure 1. While actual op amps do not have these ideal characteristics, their performance is usually sufficiently good that the circuit behavior closely approximates that of an ideal op amp in most applications.

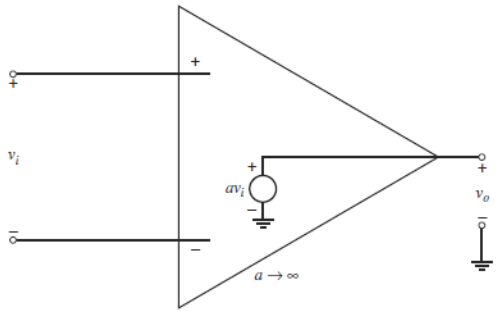

Figure 1: Ideal operational amplifier

In op amp design, bipolar transistors offer many advantages over their CMOS counterparts, such as higher transconductance for a given current, higher gain, higher speed, lower input-referred offset voltage and lower input-referred noise voltage. However, CMOS technologies have become dominant in building the digital portions of signal-processing systems because CMOS digital circuits are smaller and dissipate less power than their bipolar counterparts. To reduce system cost and increase portability, analog and digital circuits are now often integrated together, providing a strong economic incentive to use CMOS op amps.[2]

For an ideal op amp, the input impedance and the gain would be infinity. To approach these properties, in this design, we will need to design the three parts of the op amps. First part is the folded cascode op amp, which can provide extremely high gain and high input impedance. Second part is the current biasing circuit, that is because in building an op amp, to support the current biasing, a supply-independent current biasing start-up circuit is needed.[3] Third part is the voltage biasing circuit, in this circuit, we need to design the circuit so that the voltage point used in the folded cascode op amp is stable and appropriate.

2 Design Concept

In this design project, we will apply the strategy called "Divide and Conquer", or say superposition in the other word. That is, build the circuit step by step and make sure each of them are working perfectly and then add them up to a complete one.

2.1 Parameters of MOSFET

Firstly, we will need to find out the parameters of the NMOS and the PMOS such as μC_{ox}, V_{th} and λ so that we can do hand calculation to find out the approximate designing value. Since the channel length modulation will effect these parameters, so we choose a decent value of the channel length as 180nm, which is also one of the standard fabrication processes being used nowadays.

We applied the test circuit as Figure 2 to measure the properties of the MOSFETs (It is also used for NMOS testing). Table 1 shows the hand calculation result of V_{th}, μC_{ox} and λ of both NMOS and PMOS with $W = 30\mu m$ and $L = 180nm$.

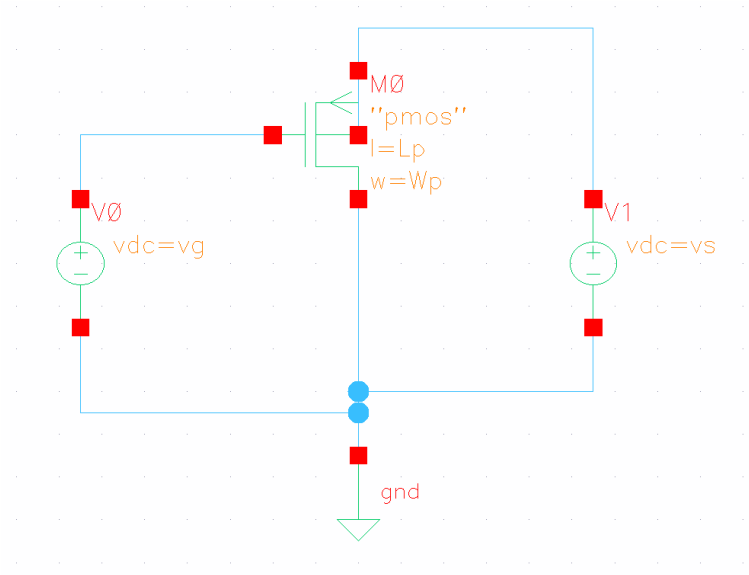

Figure 2: Parameter Test Circuit

Table 1: Parameter Extration of L=180nm, W=30μm Transistor

	V_{th} **(V)**	μC_{ox} **(mA/V^2)**	λ **(V^{-1})**	$V_{th,body}$ **(V)**
NMOS	0.390	0.280	0.086	0.440
PMOS	-0.370	0.036	-0.027	-0.450

2.2 Folded Cascode OP Amp Circuit

2.2.1 Conceptual Diagram

To meet with the requirements of gain and UGBW, we will need to design the folded cascode op amp first. A conceptual folded cascode op amp is shown in Figure 3.

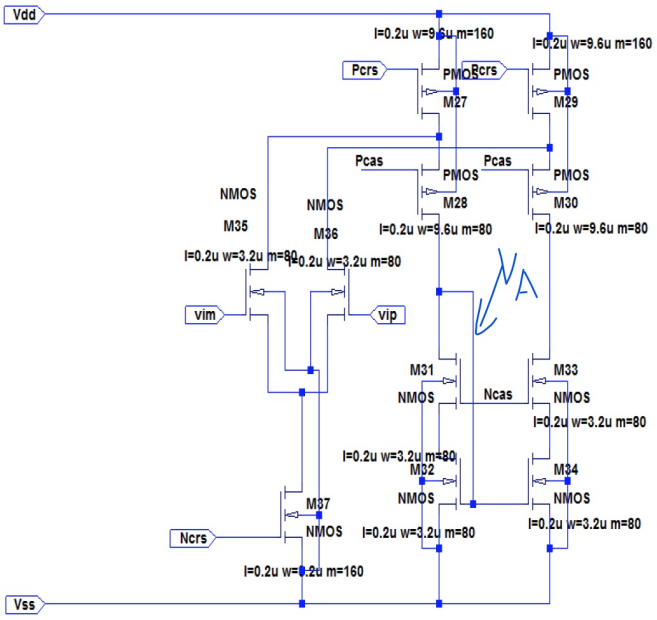

Figure 3: Conceptual Diagram of A Folded Cascode Op Amp

For a folded cascode op amp, the short-circuit transconductance and output resistance are:

$$G_M = g_{m,35}\frac{r_{o,35}}{r_{o.35} + 1/g_{m,35}} \qquad R_{out} \approx g_{m,33} r_{o,33}^2 \tag{1}$$

Then the amplification is about:

$$A_v = G_M \times R_{out} \approx g_{m,35} g_{m,33} r_{o,33}^2 \tag{2}$$

For simplicity, we set the V_{DD} as 1.6V and V_{SS} as 0V.

2.2.2 Voltage settling

For V_{PCRS}, which is decided by M27, its value is about:

$$V_{PCRS} = V_{DD} - |V_{th,p}| - |V_{dsat27}| \tag{3}$$

Since the value of V_{DD} is larger, there would be more operating space for us. In this case, the value of $|V_{dsat27}|$ is about 150mV, which is large enough to ensure that M27 is always in saturation region. Then the value of V_{PCRS} is about 1.12V. Similarly, to ensure M37 is in saturation region, we have:

$$V_{NCRS} = V_{th,n} + V_{dsat37} \tag{4}$$

With the value of V_{dsat37} as 100mV, the value of V_{NCRS} is about 500mV.

For the mid point V_A shown in Figure 3, since it connected between the gate of M32 and the drain of M31 and M28, the value of it would be very important and sensitive. In this design, we set it as 700mV, then the gate-source voltage of M32, and there will be about 700mV space to assign the drain-source voltage for M31 and M32.

After designing the value of V_A, for V_{PCAS}, we design the source of M28 as 1.15V, then the voltage of V_{PCAS} is:

$$V_{PCAS} = V_{drain,28} - |V_{th,p}| - |V_{dsat28}| \tag{5}$$

Assume the value of $|V_{dsat28}|$ is about 150mV, then the value of V_{PCAS} is about 650mV.

Similarly, for V_{NCAS}, we design the source of M31 is about 450mV, then we have:

$$V_{NCAS} = V_{source,31} + V_{th,n} + V_{dsat31} \tag{6}$$

Assume the value of V_{dsat31} is about 150mV, then the value of V_{NCAS} is about 1V.

For the DC common input, the drain of M35 and M36 is about 1.15V. To ensure both of them are in saturation, we design the value of drain of M37, which is also the source of M35 and M36 as 250mV so that both M35 and M36 will have more voltage space to ensure them are in saturation region. Then the voltage of the DC common input is:

$$V_{DC,CM} = V_{source,35} + V_{th,n} + V_{dsat35} \tag{7}$$

Assume the value of V_{dsat35} is about 100mV, then the value of $V_{DC,CM}$ is about 750mV.

2.2.3 Transistor Sizing

To adjust and optimize the circuit more easily, we decided to make the current in each branch of the differential pair as 10μA. Then for M35, M36 and M37, with the current equation for MOSFET in saturation region show below:

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W_4}{L_4}V_{dsat}^2(1+\lambda V_{ds}) \tag{8}$$

We can calculate the size of the M35, M36 and M37 as:

$$\begin{aligned}
\frac{W_{35}}{L_{35}} &\approx 19.84 \Rightarrow W_{35} = 3.57\mu m \\
\frac{W_{36}}{L_{36}} &\approx 19.84 \Rightarrow W_{36} = 3.57\mu m \\
\frac{W_{37}}{L_{37}} &\approx 11.77 \Rightarrow W_{37} = 2.13\mu m
\end{aligned} \tag{9}$$

For the two cascode branches that provide high output impedance, assume the current through them is also 10μA as well. Then for M28, M30, M31, M33, M32 and M34, we have:

$$\begin{aligned}
\frac{W_{28}}{L_{28}} &\approx 119.76 \Rightarrow W_{28} = 21.56\mu m \\
\frac{W_{30}}{L_{30}} &\approx 119.76 \Rightarrow W_{30} = 21.56\mu m \\
\frac{W_{31}}{L_{31}} &\approx 6.53 \Rightarrow W_{31} = 1.18\mu m \\
\frac{W_{33}}{L_{33}} &\approx 6.53 \Rightarrow W_{33} = 1.18\mu m \\
\frac{W_{32}}{L_{32}} &\approx 0.75 \Rightarrow W_{32} = 0.13\mu m \\
\frac{W_{34}}{L_{34}} &\approx 0.75 \Rightarrow W_{34} = 0.13\mu m
\end{aligned} \tag{10}$$

For the upper part, say M27 and M29, the current through them is 20μA, then we have:

$$\begin{aligned}
\frac{W_{27}}{L_{27}} &\approx 91.83 \Rightarrow W_{27} = 16.53\mu m \\
\frac{W_{29}}{L_{29}} &\approx 91.83 \Rightarrow W_{29} = 16.53\mu m
\end{aligned} \tag{11}$$

2.2.4 Gain Calculation

Then we use the multiplier to adjust the current go through each branch. The total current go through the folded cascode op amp is about 2mA, for the differential pair, it is about 1.7mA, and for high impedance part, it is about 0.3mA. The reason we doing so is that in Eq 2, it is proportional to the transconductance of the M35 and the channel length modulation resistance of M33. The way to increase both of them is to adjust larger percentage of the total current into the differential pair part. So the multiplier for differential pair is 170, for high impedance part is 30 and for total current part is about 100.

Then we can calculate the value of transconductance $g_{m,35}$ and the channel length modulation $r_{o,33}$ resistance.

$$\begin{aligned} g_{m,36} &= \frac{2I_{D,36}}{V_{gs,36} - V_{th}} \approx 5.66 \times 10^{-6}\ (A/V) \\ g_{m,33} &= \frac{2I_{D,33}}{V_{gs,33} - V_{th}} \approx 2.65 \times 10^{-6}\ (A/V) \\ r_{o,33} &= \frac{1}{\lambda I_{D,33}} \approx 1.45 \times 10^{5}\ (\Omega) \\ A_v &= G_M \times R_{out} \approx 3.15 \times 10^{4} \approx 90\ dB \end{aligned} \tag{12}$$

The simulation result is in Figure 4. All the transistors are in saturation mode.

2.3 4-Level Current Bias Circuit

2.3.1 Conceptual Diagram

In building a CMOS operational amplifier, to support the current biasing, a supply-independent current biasing startup circuit is needed[3]. The conceptual diagram of the 4-level current bias circuit is shown in Figure 5. To make sure that the current source more stable, say supply independence, we tried to enhance the current of the bias current, which is equal to 200μA.

2.3.2 Voltage settling

For V_{NS}, which is decided by M4, its value is:

$$V_{NS} = V_{th,n} + V_{dsat,4} \tag{13}$$

Assume the value of $V_{dsat,4}$ is about 200mV, then we have the value of V_{NS} as 600mV. Similarly, for V_{PS} we have:

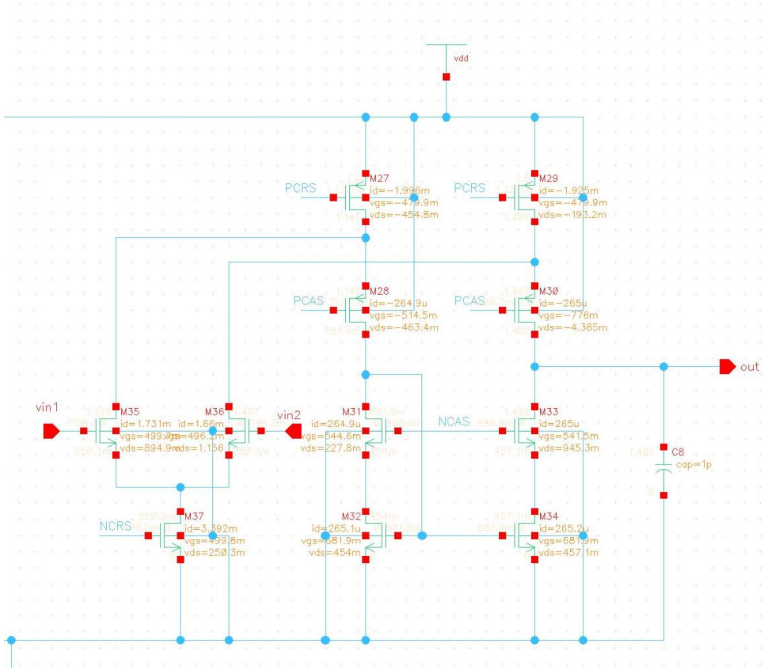

Figure 4: Simulation of Folded Cascode Op Amp

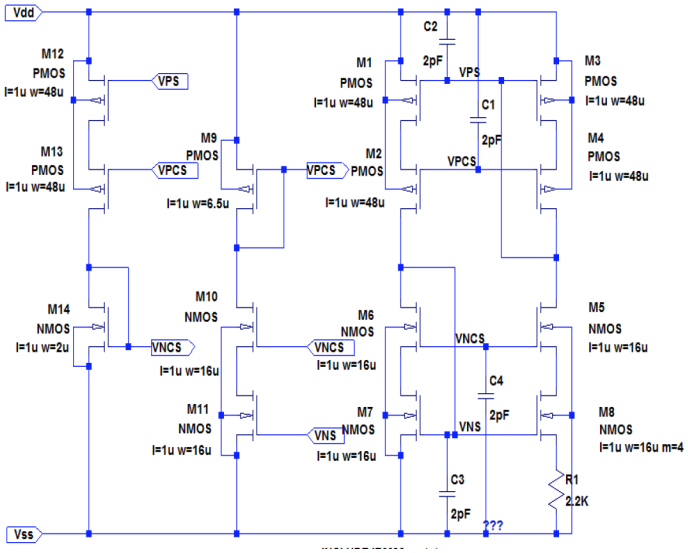

Figure 5: Conceptual Diagram of A 4-Level Current Bias Circuit

$$V_{PS} = V_{DD} - |V_{th,p}| - V_{dsat,8} \tag{14}$$

With $|V_{dsat,8}|$ as around 200mV, the value of V_{PS} is around 1V.
To make sure that M2 is in saturation mode, we have

$$\begin{aligned} V_{NS} &> V_{NCS} - V_{th,n} \\ \Rightarrow V_{NCS} &< V_{NS} + V_{th,n,body} \end{aligned} \tag{15}$$

Similarly, to make sure M5 is in saturation, we have

$$\begin{aligned} V_{source,5} - V_{PS} &> V_{source,5} - V_{PCS} - |V_{th,p,body}| \\ \Rightarrow V_{PCS} &> V_{PS} - |V_{th,p,body}| \end{aligned} \tag{16}$$

For M6 and M1, we have

$$\begin{aligned} V_{source,6} - V_{NS} &> V_{source,6} - V_{PCS} - |V_{th,p,body}|, \\ V_{PS} - V_{source,1} &> V_{NCS} - V_{source,1} - V_{th,n,body} \\ \Rightarrow V_{PCS} &> V_{NS} - |V_{th,p,body}|, \\ \Rightarrow V_{NCS} &< V_{PS} + V_{th,n,body} \end{aligned} \tag{17}$$

For the right two branches, for M10 and M13, we have

$$\begin{aligned} V_{source,10} - V_{NCS} &> V_{source,10} - V_{PCS} - |V_{th,p,body}|, \\ V_{PCS} - V_{source,1} &> V_{NCS} - V_{drain,1} - V_{th,n,body} \\ \Rightarrow V_{NCS} &< V_{PCS} + |V_{th,p,body}|, \\ \Rightarrow V_{NCS} &< V_{PCS} + V_{th,n,body} \end{aligned} \tag{18}$$

With Equation 13-18, we can conclude the constraints of V_{NS}, V_{PS}, V_{NCS} and V_{PCS} as:

$$\begin{aligned} V_{NS} &= V_{th,n} + V_{dsat,4} = 600mV, \\ V_{PS} &= V_{DD} - |V_{th,p}| - |V_{dsat,7}| = 1V, \\ V_{NCS} < V_{NS} + V_{th,n,body} &\Rightarrow V_{NCS} < 970mV, \\ V_{PCS} > V_{PS} - |V_{th,p,body}| &\Rightarrow V_{PCS} > 630V, \\ V_{NCS} - V_{PCS} &< |V_{th,p,body}| \approx 450mV \end{aligned} \tag{19}$$

Then we choose the value of V_{NS}, V_{PS}, V_{NCS} and V_{PCS} as:

$$\begin{aligned} V_{NS} &= 600mV, \\ V_{PS} &= 1V, \\ V_{NCS} &= 950mV, \\ V_{PCS} &= 700mV \end{aligned} \tag{20}$$

2.3.3 Transistor settling

Bottom Part

For the bottom part, firstly we will decide the size of M4 since we've already known the V_{gs} and V_{ds} of M4. With 8, we have:

$$\frac{W_4}{L_4} \approx 32.39 \Rightarrow W_4 \approx 5.83\mu m \tag{21}$$

For M3, since the current is about 200μA, to reduce the impact of the resistor R_0, its value of R_0 is set as around 250Ω. Then we have the equation of the sizing of M3:

$$\begin{aligned} I_{out} &= \frac{2}{\mu_n C_{ox}\frac{W_4}{L_4}} \cdot \frac{1}{R^2}(1 - \sqrt{\frac{W_4}{L_4}/\frac{W_3}{L_3}})^2 \\ \Rightarrow \quad \frac{W_3}{L_3} &\approx 55.79 \Rightarrow W_3 \approx 10.04\mu m \end{aligned} \tag{22}$$

To make sure both M1 and M2 are in saturation region, approximately we have:

$$\begin{aligned} \frac{W_1}{L_1} &\approx 118.06 \Rightarrow W_1 = 21.25\mu m, \\ \frac{W_2}{L_2} &\approx 27.01 \Rightarrow W_2 = 4.86\mu m \end{aligned} \tag{23}$$

Upper Part

For the PMOS part, it is much more easy to handle since there is no resistance in the circuit. Firstly we will decide the size of M7 and M8 since we've already known the V_{gs} and V_{ds} of them. With 8, we have:

$$\begin{aligned} \frac{W_7}{L_7} &\approx 210.04 \Rightarrow W_7 = 37.81\mu m, \\ \frac{W_8}{L_8} &\approx 210.04 \Rightarrow W_8 = 37.81\mu m \end{aligned} \tag{24}$$

And to make sure that both M5 and M6 are in saturation region, approximately we have:

$$\begin{aligned} \frac{W_5}{L_5} &\approx 657.46 \Rightarrow W_5 = 118.34\mu m, \\ \frac{W_6}{L_6} &\approx 3086.42 \Rightarrow W_6 = 555.56\mu m \end{aligned} \tag{25}$$

Feedback & Bias Part

The right two branches are for biasing the voltage of V_{NCS} and V_{PCS}. For the left branch, M11 is for biasing the value of V_{NCS}, and the other two, say M9 and M10 are for feedback of V_{PS} and V_{PCS}. Similarly, for the right branch, M12 is for biasing the value of V_{PCS}, and M13 and M14 are for feedback of V_{NCS} and V_{NS}.

For M11 and M12, with the value of V_{NCS} and V_{PCS} decided as 950mV and 700mV, we can calculate the value of $\frac{W_{11}}{L_{11}}$ and $\frac{W_{12}}{L_{12}}$ with Eq 8.

$$\begin{aligned} \frac{W_{11}}{L_{11}} &\approx 4.56 \Rightarrow W_{11} = 820.8nm, \\ \frac{W_{12}}{L_{12}} &\approx 39.56 \Rightarrow W_{12} = 7.12\mu m \end{aligned} \tag{26}$$

For M9, M10, M13, M14, to make sure all of them are in saturation region, approximately we have:

$$\begin{aligned} \frac{W_9}{L_9} &\approx 210.04 \Rightarrow W_9 = 37.81\mu m, \\ \frac{W_{10}}{L_{10}} &\approx 493.83 \Rightarrow W_{10} = 88.89\mu m \\ \frac{W_{13}}{L_{13}} &\approx 84.53 \Rightarrow W_{13} = 15.22\mu m, \\ \frac{W_{14}}{L_{14}} &\approx 32.39 \Rightarrow W_{14} = 5.83\mu m \end{aligned} \tag{27}$$

After some adjustment, the simulation result is shown in Figure 6. For each biasing branch, we designed the sizing of the transistors so that the current go through each branch is very close to 200μA, which will have a better feedback performance in stabling the biasing voltage in the current mirror, and all the transistors are in saturation mode.

2.4 4-Level Voltage Bias Circuit

2.4.1 Conceptual Diagram

In building folded cascode op amp part, we used the biasing voltage V_{NCRS}, V_{NCAS},V_{PCRS} and V_{PCAS}. To get a stable voltage biasing, a supply-independent voltage biasing circuit is needed. The conceptual diagram of the 4-level voltage biasing circuit is shown in Figure 7.

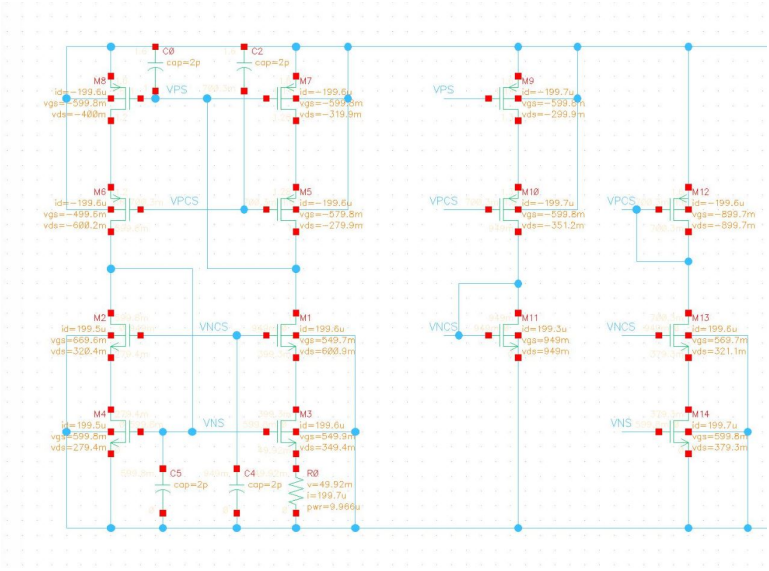

Figure 6: Simulation of 4-Level Current Bias Circuit

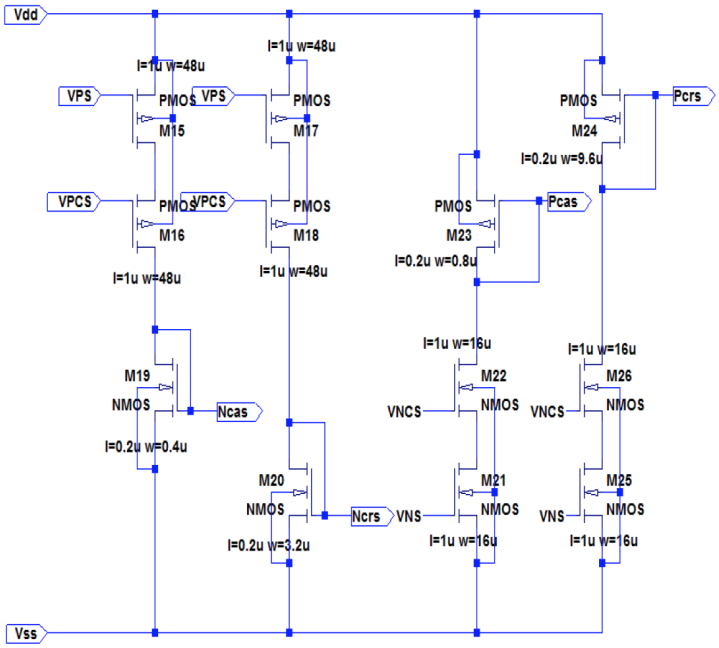

Figure 7: Conceptual Diagram of A 4-Level Voltage Bias Circuit

2.4.2 Transistor Sizing

Since we've already had the value of V_{NS}, V_{PS}, V_{NCS}, V_{NCS}, V_{NCAS}, V_{NCRS}, V_{PCAS} and V_{PCRS}, we just need to do the sizing design.

Because of the similarity, M22 and M26 would have the same size, M25 and M21 would be the same, M15 and M17 are the same, and M16 and M18 are the same. With the saturation current 8, we have:

$$\begin{aligned}
\frac{W_{15}}{L_{15}} = \frac{W_{17}}{L_{17}} \approx 210.04 \Rightarrow W_{15} = W_{17} = 37.81\mu m, \\
\frac{W_{16}}{L_{16}} = \frac{W_{18}}{L_{18}} \approx 493.87 \Rightarrow W_{16} = W_{19} = 88.89\mu m, \\
\frac{W_{21}}{L_{21}} = \frac{W_{25}}{L_{25}} \approx 32.39 \Rightarrow W_{21} = W_{25} = 5.83\mu m, \\
\frac{W_{22}}{L_{22}} = \frac{W_{26}}{L_{26}} \approx 84.53 \Rightarrow W_{22} = W_{16} = 15.22\mu m
\end{aligned} \tag{28}$$

Then we have the drain voltage of M19, M20, M23 and M24, then we can calculate size of them:

$$\begin{aligned}
\frac{W_{19}}{L_{19}} \approx 3.86 \Rightarrow W_{19} = 694.8nm, \\
\frac{W_{20}}{L_{20}} \approx 118.06 \Rightarrow W_{20} = 21.25\mu m, \\
\frac{W_{23}}{L_{23}} \approx 30.86 \Rightarrow W_{23} = 5.55\mu m, \\
\frac{W_{24}}{L_{24}} \approx 918.27 \Rightarrow W_{24} = 165.29\mu m
\end{aligned} \tag{29}$$

Figure 8 shows the simulation result of the 4-level voltage bias circuit, and all the transistors are in saturation mode.

2.5 Complete Circuit

2.5.1 DC Simulation

Figure 9 shows the DC simulation result of the complete circuit, and all the transistors are in saturation mode.

3 Simulation Result & Conclusion

All the open loop testbench are based on the circuit shown in Figure 10.

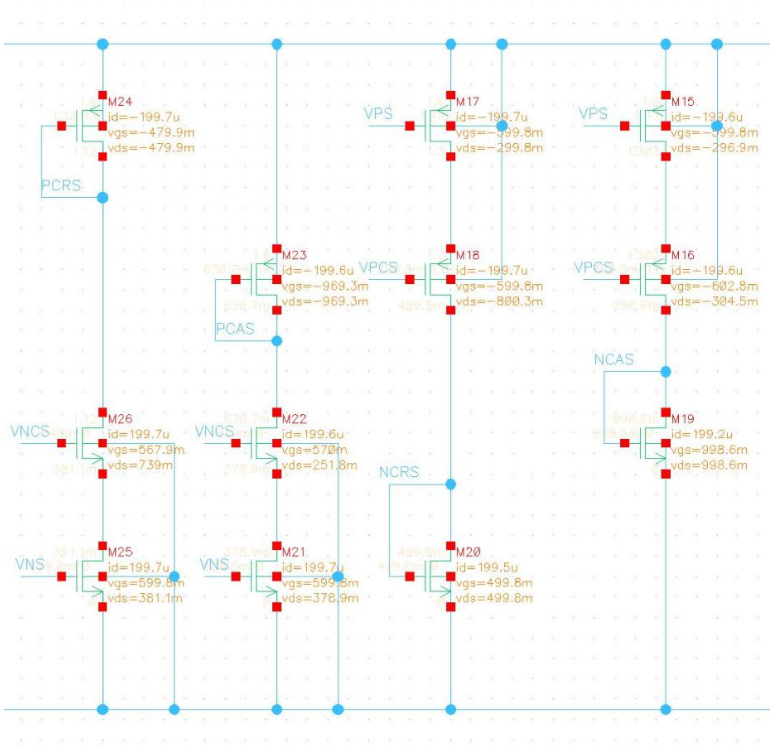

Figure 8: Simulation of 4-Level Voltage Bias Circuit

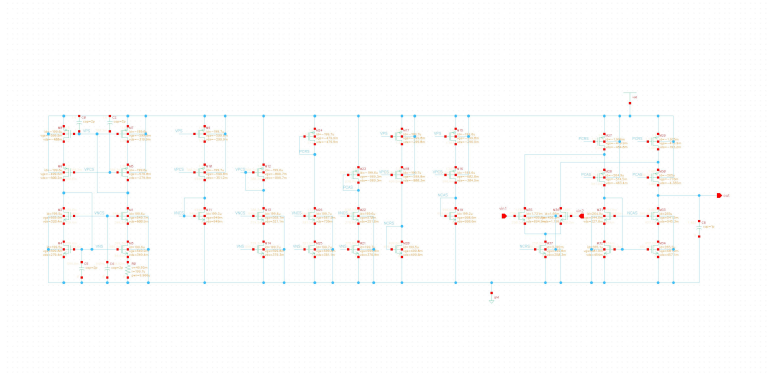

Figure 9: DC Simulation of Complete Circuit

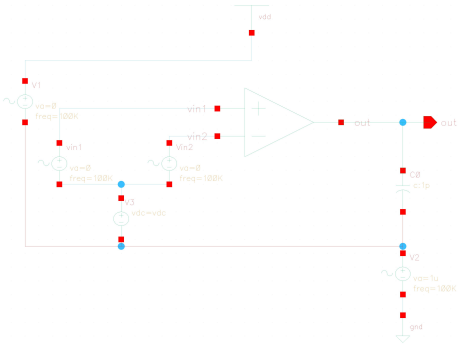

Figure 10: Open loop Testbench of Complete Folded Cascode Op Amp

3.1 Open Loop Gain & Close Loop Phase Margin

Figure 11 shows the AC simulation result of the complete circuit. The open loop DC gain A_{DM} is about 89.7dB, and the -3dB frequency ω_{-3dB} is about 400KHz. The unity-gain bandwidth is about 1.7GHz, which is larger than the requirement 1GHz. The close loop phase margin ϕ_{PM} is 65.6°.

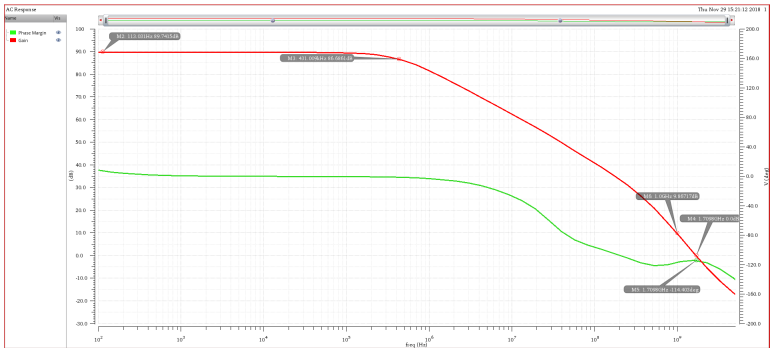

Figure 11: AC Simulation of Complete Folded Cascode Op Amp

The transient response of the circuit at 100KHz is shown in Figure 12.

3.2 Input Common Mode Range

For input common mode range (ICMR), in Figure 10, we keep both the input small signal and sweep the common mode dc input and see when the circuit is still working properly. Figure 13 shows the simulation result. The two dash lines are the cases that when the circuit do not have enough gain, which is at 0.4V and 1.8V. And the two dot lines are the cases that when the circuit exactly have the gain higher than 70dB, which is 0.45V and 1.75V. Then the input common mode range (ICMR) is about 1.3V.

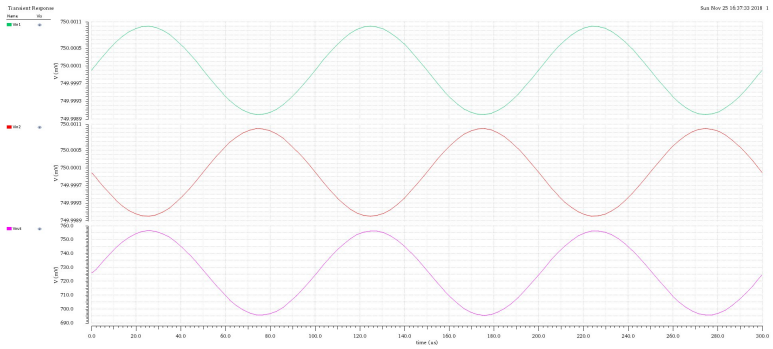

Figure 12: Transient Simulation of Complete Folded Cascode Op Amp

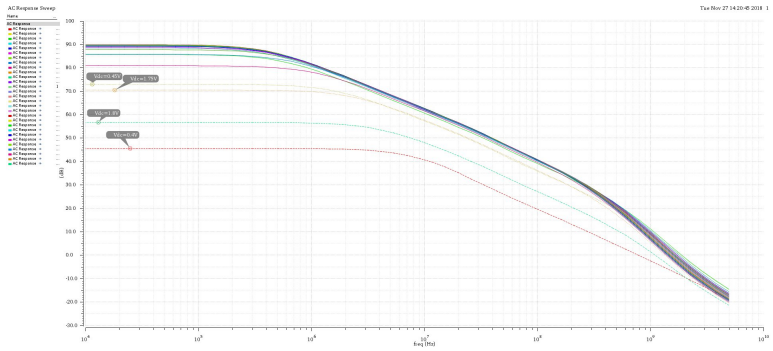

Figure 13: ICMR Simulation of Complete Folded Cascode Op Amp

3.3 Positive/Negative Power Supply Rejection Ratio

To find the power supply rejection ratio, we will need to calculate the open loop gain and the power supply gain, and then follow the definition of PSRR as

$$PSRR = \frac{A_{DM}}{A_{PS}} \tag{30}$$

3.3.1 Positive Power Supply Rejection Ratio

Transient Response

For positive power supply rejection ratio, in Figure 10, a sinusoidal waveform is given to the power supply V_{DD}. The transient response at 100KHz is shown in Figure 14.

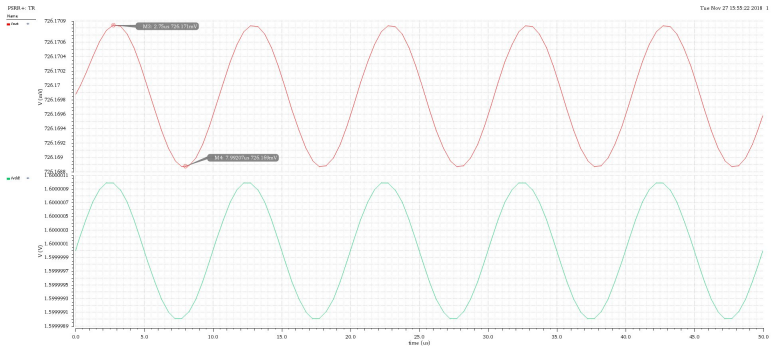

Figure 14: Positive PSRR Transient Simulation of Complete Folded Cascode Op Amp

Positive Power Supply Gain

Figure 15 shows the positive power supply gain. For open loop DC case, it is about -35.9dB.

Positive PSRR

With the definition given in Eq 30, the positive PSRR should be equal to the open loop differential gain divided by the positive power supply gain, which is about 125.6. And in Figure 16, the value of it is about 125.5dB, which is very close to the estimated value.

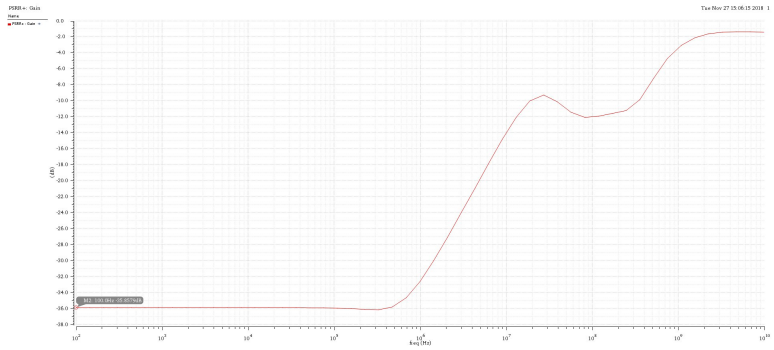

Figure 15: Positive PSRR Gain of Complete Folded Cascode Op Amp

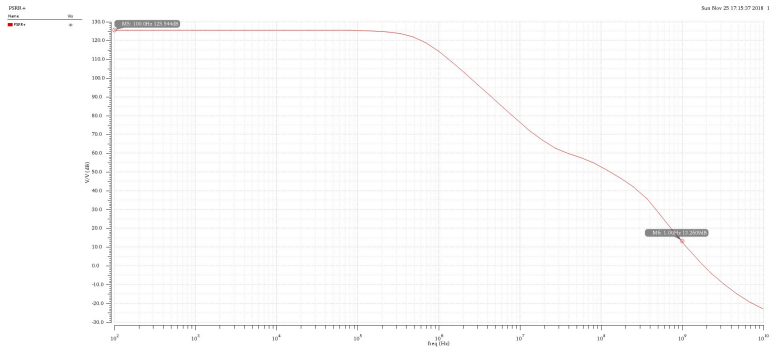

Figure 16: Positive PSRR of Complete Folded Cascode Op Amp

3.3.2 Negative Power Supply Rejection Ratio

Transient Response

For negative power supply rejection ratio, in Figure 10, a sinusoidal waveform is given to the power supply V_{SS}. The transient response at 100KHz is shown in Figure 17.

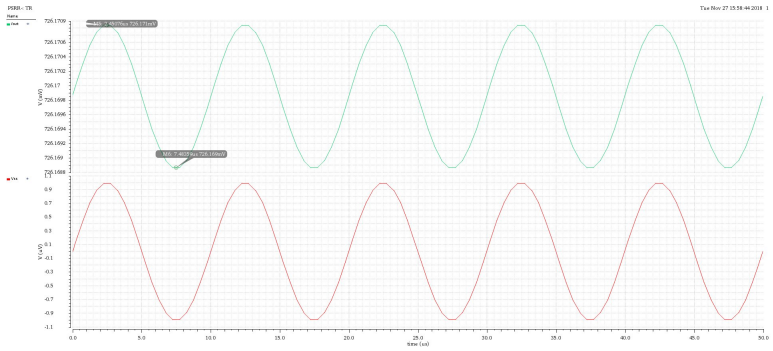

Figure 17: Negative PSRR Transient Simulation of Complete Folded Cascode Op Amp

Negative Power Supply Gain

Figure 18 shows the negative power supply gain. For open loop DC case, it is about -21.1dB.

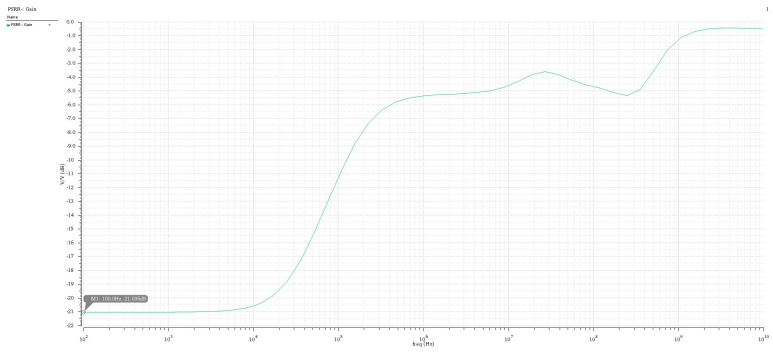

Figure 18: Negative PSRR Gain of Complete Folded Cascode Op Amp

Negative PSRR

With the definition given in Eq 30, the negative PSRR should be equal to the open loop differential gain divided by the negative power supply

gain, which is about 110.8. And in Figure 19, the value of it is about 110.7dB, which is very close to the estimated value.

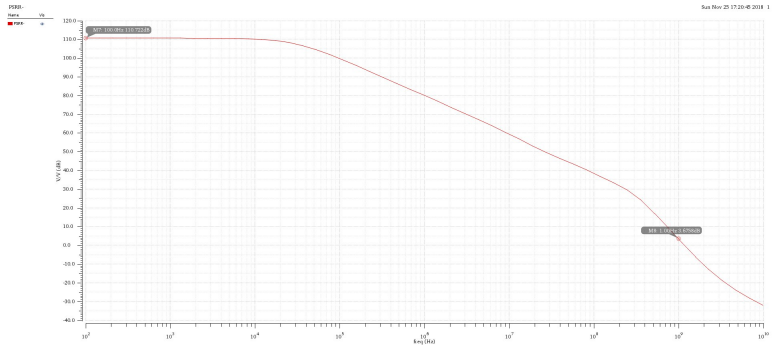

Figure 19: Negative PSRR of Complete Folded Cascode Op Amp

3.4 Common Mode Rejection Ratio

3.4.1 Definition of CMRR

The op amp common-mode rejection ratio (CMRR) is the ratio of the common mode gain to differential mode gain. Then to find its we will need to find out the common mode gain of the op amp. The way we do that is applying the small signal with identical phase settling to the differential input and see how the output would response to this common mode input. The equation of CMRR is defined as:

$$CMRR = \frac{A_{DM}}{A_{CM}} \tag{31}$$

3.4.2 Transient Response

Figure 20 shows the transient response of output with common mode input.

3.4.3 Common Mode Gain

Figure 21 shows the common mode gain. For open loop DC case, it is about -19.6dB.

3.4.4 CMRR

With the definition given in Eq 31, the value of CMRR should be equal to the open loop differential gain divided by the common mode gain, which

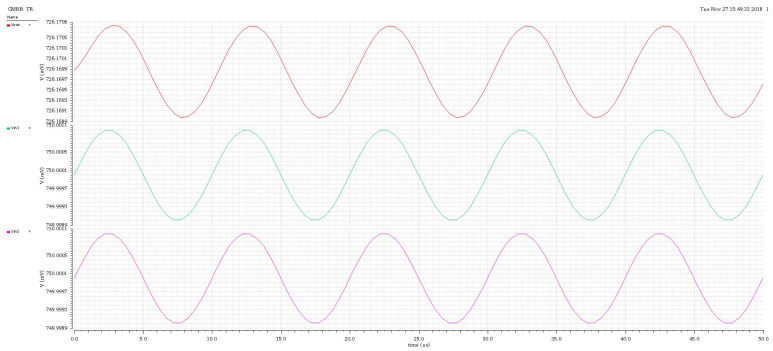

Figure 20: CMRR Transient Simulation of Complete Folded Cascode Op Amp

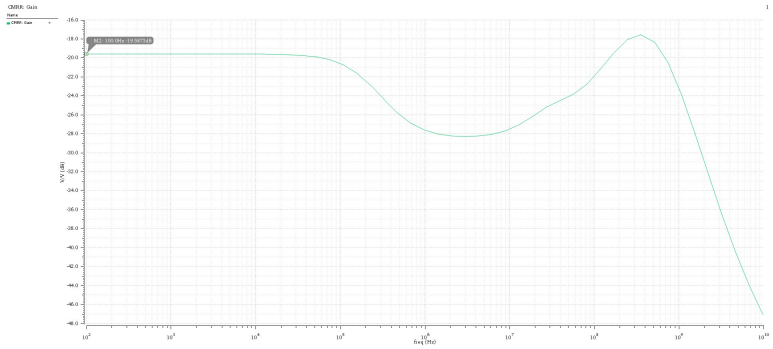

Figure 21: Common ModeGain of Complete Folded Cascode Op Amp

is about 109.3. And in Figure 22, the value of it is about 109.3dB, which is very close to the estimated value.

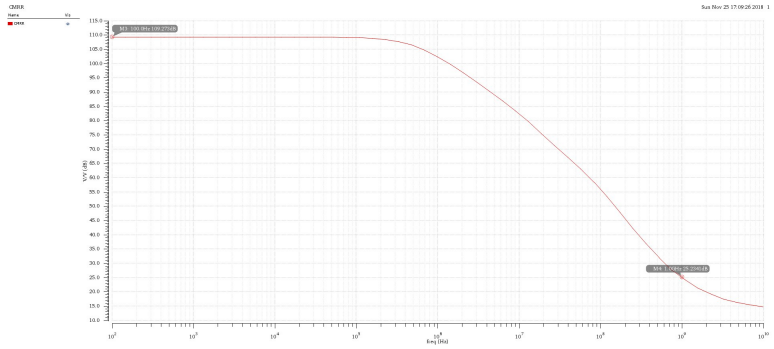

Figure 22: CMRR of Complete Folded Cascode Op Amp

3.5 Positive/Negative Slew Rate

In electronics, slew rate is defined as the change of voltage or current, or any other electrical quantity, per unit of time. In most cases, we want higher slew rate so that the circuit has less delay and better performance. For slew rate testing, in Figure 10, an abrupt pulse is given to the input and the we can see the output to find out the slew rate of the op amp.

3.5.1 Positive Slew Rate

Figure 23 shows the simulation result of the slew rate. For the rising pulse, the slope of the rising edge is about 0.175V/ns.

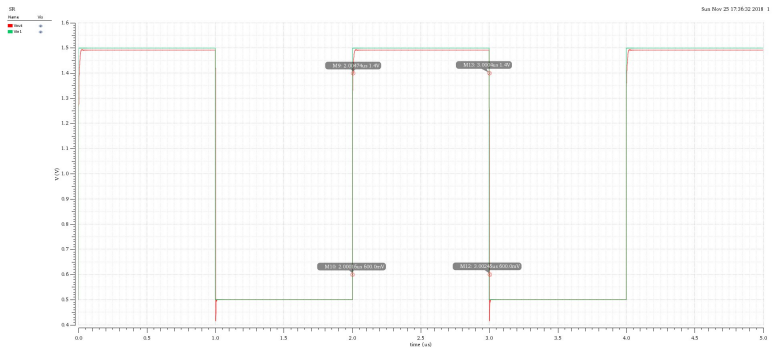

Figure 23: Slew Rate of Complete Folded Cascode Op Amp

3.5.2 Negative Slew Rate

From Figure 23, for the falling pulse, the slope of the falling edge is about -0.390V/ns.

3.6 Positive/Negative Settling Time

The settling time is the time that the output can reach to the stable value since in some cases, the output of the system would keep oscillating and take a long time to converge to a stable value. In most cases, we want to have a smaller settling time and to avoid the oscillating of the output signal. For settling time test, we just follow the testbench in slew rate test.

3.6.1 Positive Settling Time

Figure 24 shows the simulation result of the positive settling time test. For the rising pulse, the output does not have much oscillation, then the positive settling is about 35.5ns.

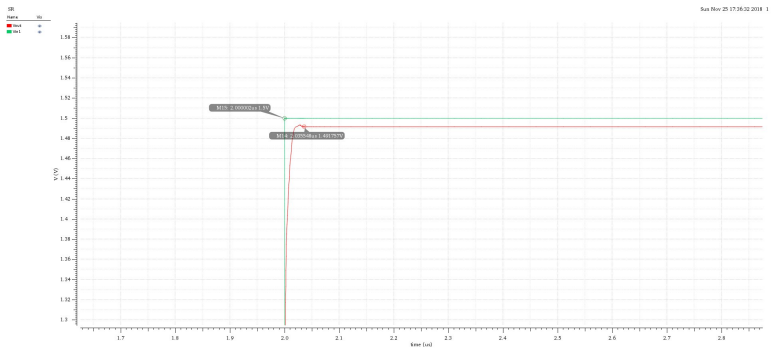

Figure 24: Positive Settling Time of Complete Folded Cascode Op Amp

3.6.2 Negative Settling Time

Figure 25 shows the simulation result of the negative settling time test. For the falling pulse, the output has some oscillation, and the negative settling is about 15.7ns.

3.7 Power Analysis

Figure 9 shows the DC simulation of the circuit. The voltage supply V_{DD} is 1.6V, and the total current is about 4.4mA. Then the total power consumption is:

$$P = V_{DD} \times I = 7.04\ mW \tag{32}$$

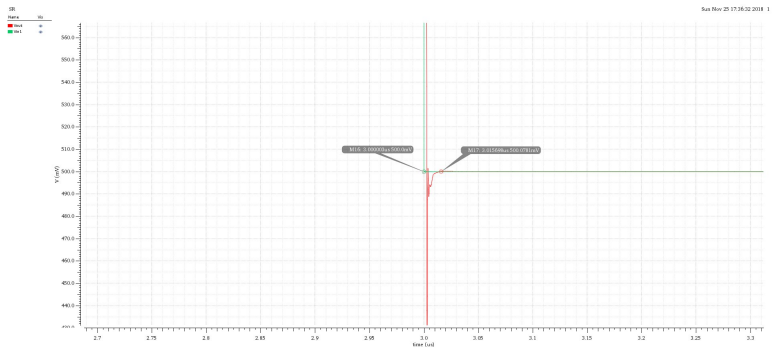

Figure 25: Negative Settling Time of Complete Folded Cascode Op Amp

3.8 Conclusion

3.8.1 Performance Analysis

Table 2: Performance of Folded Cascode Op Amp

Parameter Description	**Desired**	**Achieved**	**Unit**
Power Supply (V_{DD})	0.8-1.6	1.6	V
Ground Supply (V_{SS})	0	0	V
Output Load (C_L)	1	1	pF
Op Amp Open Loop DC Gain (A_v)	70	89.7	dB
Phase Margin (ϕ)	>65	65.6	°
Positive Settling Time	<5	35.5	ns
Negative Settling Time	<5	15.7	ns
Supply Current Consumption (I_{DD})	-	4.4	mA
Power Consumption ($V_{DD} \times I_{DD}$)	-	7.04	mW
Positive Slew Rate (SR+)	>1	0.175	V/ns
Negative Slew Rate (SR-)	>1	0.390	V/ns
Input Common Mode Range (ICMR)	-	1.3	V
Positive Power Supply Rejection Ratio (PSRR+)	>60	125.5	dB
Negative Power Supply Rejection Ratio (PSRR-)	>60	110.7	dB
Common Mode Rejection Ratio (PSRR-)	>60	109.3	dB

3.8.2 Voltage settling

The voltage setting for some important points are shwon in Table 3.

Table 3: Biasing Voltage: Hand Calculation vs Simulation

	V_{NS} **(mV)**	V_{NCS} **(mV)**	V_{PS} **(mV)**	V_{PCS} **(mV)**
Hand Calculation	600	950	1000	700
Simulation	599.8	949.0	1000.2	700.3
	V_{NCAS} **(mV)**	V_{NCRS} **(mV)**	V_{PCAS} **(mV)**	V_{PCRS} **(mV)**
Hand Calculation	1000	500	650	1120
Simulation	998.8	499.8	650.7	1120.0

3.8.3 Sizing of Transistors & Some Details

To make the report more readable, the sizing details of transistors are divided into three part: Current Biasing Circuit, Voltage Biasing Circuit and Folded Cascode Op Amp. All the transistors have the channel length L as 180nm.

Current Biasing Circuit

The sizing details of each transistor of current biasing circuit are shown in Table 4.

Voltage Biasing Circuit

The sizing details of each transistor of voltage biasing circuit are shown in Table 5.

Folded Cascode Op Amp

The sizing details of each transistor of the folded cascode op amp are shown in Table 6. For M27 and M29, the multiplier is 100; for M28, M30, M31, M32, M33, M34, the multiplier is 30; for M35, M36, M37, the multiplier is 170.

Table 4: Sizing of Current Biasing Circuit: Hand Calculation vs Simulation

	M_1	M_2	M_3	M_4	M_5	M_6	M_7
$\frac{W}{L}$(Hand)	118.06	27.01	55.79	32.39	657.46	3086.42	210.04
$\frac{W}{L}$(Simu)	334.17	36.28	69.33	31.67	641.67	3204.44	212.39
$W\ (\mu m)$(Hand)	21.25	4.86	10.04	5.83	118.34	555.56	37.81
$W\ (\mu m)$(Simu)	60.15	6.53	12.48	5.70	115.50	576.80	38.23
$I\ (\mu A)$(Hand)	200	200	200	200	200	200	200
$I\ (\mu A)$(Simu)	199.6	199.5	199.6	199.5	199.6	199.6	199.5
	M_8	M_9	M_{10}	M_{11}	M_{12}	M_{13}	M_{14}
$\frac{W}{L}$(Hand)	210.04	210.04	493.83	4.56	39.56	84.53	32.39
$\frac{W}{L}$(Simu)	215.89	212.22	459.44	4.33	37.72	218.17	31.33
$W\ (\mu m)$(Hand)	37.81	37.81	88.89	0.82	7.12	15.22	5.83
$W\ (\mu m)$(Simu)	37.86	38.38	82.70	0.78	6.79	39.27	5.64
$I\ (\mu A)$(Hand)	200	200	200	200	200	200	200
$I\ (\mu A)$(Simu)	199.6	199.7	199.7	199.3	199.6	199.6	199.7

Table 5: Sizing of Current Biasing Circuit: Hand Calculation vs Simulation

	M_{15}	M_{16}	M_{17}	M_{18}	M_{19}	M_{20}
$\frac{W}{L}$(Hand)	210.04	493.87	210.04	493.87	3.86	118.06
$\frac{W}{L}$(Simu)	213.22	441.11	213.22	441.11	3.78	114.83
$W\ (\mu m)$(Hand)	37.81	88.89	37.81	88.89	0.69	21.25
$W\ (\mu m)$(Simu)	38.38	79.40	38.38	79.40	0.68	20.67
$I\ (\mu A)$(Hand)	200	200	200	200	200	200
$I\ (\mu A)$(Simu)	199.6	199.6	199.7	199.7	199.2	199.5
	M_{21}	M_{22}	M_{23}	M_{24}	M_{25}	M_{26}
$\frac{W}{L}$(Hand)	32.39	84.53	30.86	918.27	32.39	84.53
$\frac{W}{L}$(Simu)	31.33	218.17	30.06	913.89	31.33	218.17
$W\ (\mu m)$(Hand)	5.83	15.22	5.55	165.29	5.83	15.22
$W\ (\mu m)$(Simu)	5.64	39.27	5.41	164.50	5.64	39.27
$I\ (\mu A)$(Hand)	200	200	200	200	200	200
$I\ (\mu A)$(Simu)	199.7	199.6	199.6	199.7	199.7	199.7

Table 6: Sizing of Folded Cascode Op Amp: Hand Calculation vs Simulation

	M_{27}	M_{28}	M_{29}	M_{30}	M_{31}	M_{32}
$\frac{W}{L}$(Hand)	91.83	119.76	91.83	119.76	6.53	0.75
$\frac{W}{L}$(Simu)	91.67	135.28	91.67	135.28	22.22	0.72
$W\ (\mu m)$(Hand)	16.53	21.56	16.53	21.56	1.18	0.13
$W\ (\mu m)$(Simu)	16.50	24.35	16.50	24.35	4.00	0.13
$I\ (\mu A)$(Hand)	2000	300	2000	300	300	300
$I\ (\mu A)$(Simu)	1996.0	264.9	1925.0	265.0	264.9	265.1
	M_{33}	M_{34}	M_{35}	M_{36}	M_{37}	
$\frac{W}{L}$(Hand)	6.53	0.75	19.84	19.84	11.77	
$\frac{W}{L}$(Simu)	22.22	0.72	20.26	20.06	11.83	
$W\ (\mu m)$(Hand)	1.18	0.13	3.57	3.57	2.13	
$W\ (\mu m)$(Simu)	4.00	0.13	3.61	3.61	2.13	
$I\ (\mu A)$(Hand)	300	300	1700	1700	3400	
$I\ (\mu A)$(Simu)	265.0	265.2	1731.0	1660.0	3392.0	

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2. Paul R Gray, Paul Hurst, Robert G Meyer, and Stephen Lewis. *Analysis and design of analog integrated circuits*. Wiley, 2001.

3. A. Boni. Op-amps and startup circuits for cmos bandgap references with near 1-v supply. *IEEE Journal of Solid-State Circuits*, 37(10):1339–1343, Oct 2002.