University of Southern California
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Solid State Processing and Integrated Circuit Laboratory
Electrical Characterizatoin of IC Devices
Final Report

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List of Nomenclatures

Resistor

ρ: Resistivity of the material $(\Omega \cdot m)$
L: Length of the block (cm)
W: Width of the block (cm)
A: Area of cross section of the block (cm^2)
t: Thickness of the block (cm)
R_{sh}: Sheet Resistance of the block $(\Omega/\square)$
$(\frac{L}{W})_{eff}$: Effective number of squares
d_i: Distance between $i\ th$ contact and $i+1\ th$ contact (cm)
R_T: Total resistance (Ω)
R_m: Resistance due to the contact metal (Ω)
R_C: Resistance due to the metal-semiconductor contact (Ω)
R_S: Resistance of the doped layer (Ω)

PN Diode

W: Width of depletion region (cm)
x_n: Width of depletion region in n-type part (cm)
x_p: Width of depletion region in p-type part (cm)
N_A: Doping concentration of acceptor (cm^{-3})
N_D: Doping concentration of donor (cm^{-3})
V_a: Externally applied voltage source (V)
V_{bi}: Built-in potential (V)
k: Boltzmann constant (eV/K)
T: Room temperature (K)
q: Elementary charge (C)
n_i: Intrinsic carrier concentration of Si at 300K (cm^{-3})
I: Measured current (A)
I_0: Reverse saturation current (A)
n: Ideality factor

MOS Capacitor

Φ_m: Metal work function (eV)
Φ_s: Semiconductor work function (eV)
χ: Electron affinity (V)
C_{SiO_2}: Capacitance of SiO_2 (F)
ϵ_{ox}: Oxide (SiO_2) relative permittivity
ϵ_0: Permittivity of the free space (F/cm)
A: Area of the capacitor (cm^2)
t_{ox}: Oxide thickness (cm)
C_{Si}: Capacitance of Si (F)
C_{sf}: Capacitance of series C_{Si} and C_{SiO_2} (F)
ϕ_f: Fermi function (V)
N_{sub}: Number of electrons in substrate
V_{FB}: Flat-band voltage (V)
C_{FB}: Flat-band capacitance (F)
L_d: Deby length (cm)
N_f: Number of charges per unit area of the capacitor (C/cm^2)
Q_{ss}: Number of charges per unit area of the capacitor (C/cm^2)

MOSFET

I_{ds}: Drain-to-source current (A)
$\bar{\mu}$: Average mobility of carriers in the channel ($cm^2/(V \cdot s)$)
C_0: Capacitance per area of the MOS structure (F/cm^2)
W: MOSFET width (μm)
L: MOSFET gate length (μm)
V_{gs}: Gate-to=source voltage (V)
V_{th}: Threshold voltage (V)
V_{ds}: Drain-to-source voltage (V)
$V_{ds,sat}$: Saturation drain-to-source voltage (V)
$I_{ds,sat}$: Saturation drain-to source current (A)
v_S: Saturation velocity (cm/s)
g_m: Transconductance (A/V)
g_d: Output conductance: (A/V)
V_{SW}: Voltage swing (V)
g_c: Channel conductance (A/V)
μ_{lin}: Carrier mobility in linear regime ($cm^2/(V \cdot s)$)

1. Abstract

This report firstly gives the theoretical details of how to calculate physical parameters of resistors, PN diode, capacitors and MOSFETs. The calculation result of each type of device of wafer is given. The wafer is fabricated in EE504 Lab session. In next part, the reasons of unexpected data and phenomenon are discussed. In the last part, the conclusion about EE504L class and lab experience is given.

2. Introduction

When talking about the trend in the development of electronic products in recent decades, Moore's law would be the first thing that people would think of. Its core content is the complexity of integrated circuits, with respect to minimum component cost, doubles every 18 to 24 months. For example, in 1987 the revenue of semiconductor industry is 33 billion dollars, however, in 2017 it has been already 408 billion dollars which is more than 10 times bigger than 1987.

However, during the development of electronic industry, bottlenecks appeared in fabrication process, Moore's law was challenged. To overcome these obstacles, some advanced fabrication process were developed, for instance, thermal oxidation, ion implantation, photolithography and so on. All these techniques are applied in this 504L lab session[3].

This report will give the theoretical method to measure some parameters of resistors, PN diodes, MOS capacitors and MOSFETs in Section 3. In Section 4, experimental results and calculations based on theorems are given. In Section 5, the reasons of unexpected data and phenomenon are discussed. And in last section, the conclusion about EE504L class and lab experience is given.

3. Theory

3.1 Resistor Measurements

3.1.1 Sheet Resistor Measurement

The resistance R of a rectangular block of uniformly doped material is given by:

$$R = \rho \cdot \frac{L}{A} = \rho \cdot \frac{L}{W \cdot t} = R_{sh} \cdot (\frac{L}{W})_{eff} \tag{3.1}$$

where
ρ is the resistivity of the material $(\Omega \cdot m)$.
L is the length of the block (cm).
W is the width of the block (cm).
A is the area of cross section of the block (cm^2).
t is the thickness of the block (cm).
R_{sh} is the sheet Resistance of the block $(\Omega/\Box)$.
$(\frac{L}{W})_{eff}$ is the effective number of squares.

The most commonly used techniques in industrial environment are the Transmission Line Measurement (TLM) and Transfer Line Method (also TLM).

3.1.2 Transmission Line Measurement

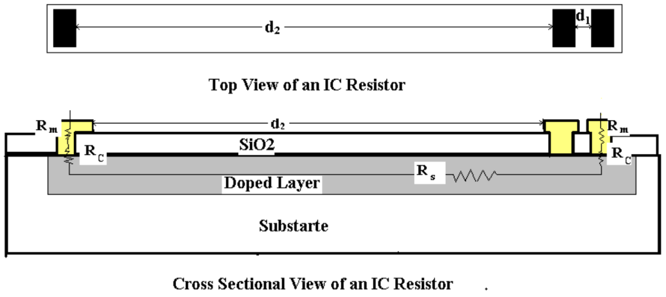

Figure 3.1: *View of IC Resistor[1]*

Figure 3.1, 3.2 show that the total resistance (R_T) measured on the scope is sum of the resistance due to the wire&probe tips (usually small and neglected), resistance due to

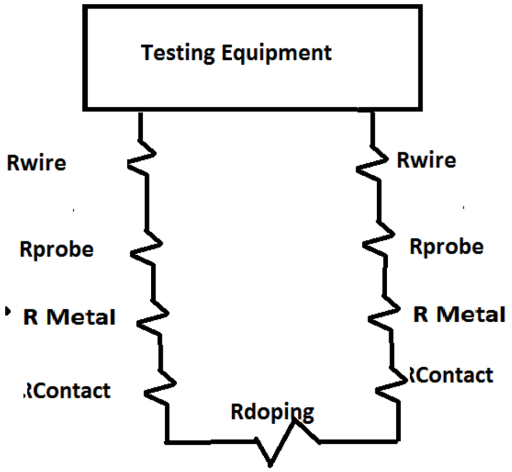

Figure 3.2: *Resistor Circuit*

the contact metal (R_m), resistance due to the metal-semiconductor contact (R_C) and the resistance of the doped layer (R_S):

$$R_T = 2R_m + 2R_C + R_S \tag{3.2}$$

Since R_m value compared R_C and R_S is small and we usually neglect that, which results in:

$$\begin{aligned} R_T &= 2R_C + R_S \\ where \qquad R_S &= R_{sh} \cdot \frac{d}{A} \end{aligned} \tag{3.3}$$

Using d_1 and d_2 and their corresponding measured total resistance of R_{T1} and R_{T2} we obtain:

$$\begin{aligned} R_{T1} &= 2R_C + R_{sh} \cdot \frac{d_1}{A} \\ R_{T2} &= 2R_C + R_{sh} \cdot \frac{d_2}{A} \end{aligned} \tag{3.4}$$

If we solve the above system for R_C, we obtain:

$$\begin{aligned} R_C &= (R_{T1} \cdot d_2 - R_{T2} \cdot d_1)/2(d_1 - d_2) \\ R_{sh} &= A(R_{T1} - R_{T2})/(d_1 - d_2) \end{aligned} \tag{3.5}$$

The disadvantage of this method for finding R_{sh} is that the A or the cross sectional area of the carrier flow in the IC resistor is needed and that depends on the junction depth (t) of the diffused layer at the end of the process, and we usually do not have this number available. That is why the Transmission Line Measurement (TLM) is used more commonly in which we can extract both R_C and R_m simultaneously without much trouble.

3.1.3 Transfer Line Method

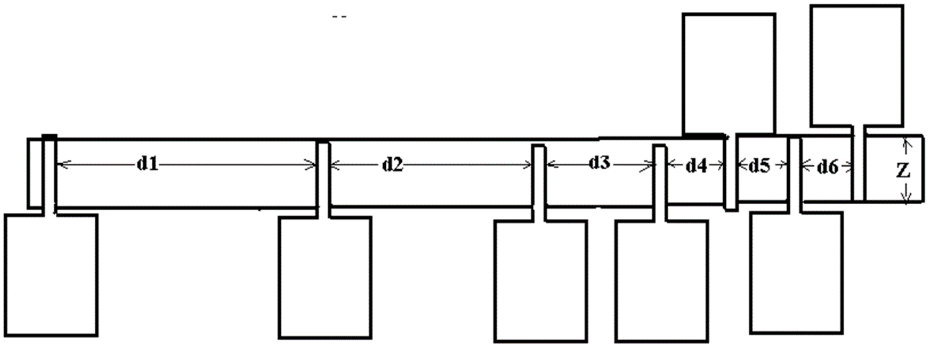

Figure 3.3: *Transfer line method test structure*

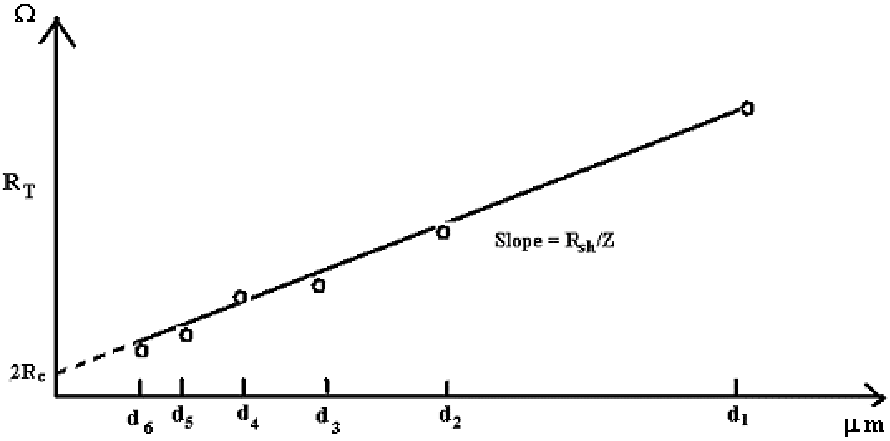

Figure 3.4: *Data Plot of TLM (R_T vs. d)*

In Figure 3.3 and 3.4, the slope is:

$$Slope = R_{sh}/Z \tag{3.6}$$

We can get R_{sh} by dividing the slope by Z (width).

3.1.4 IC Resistors

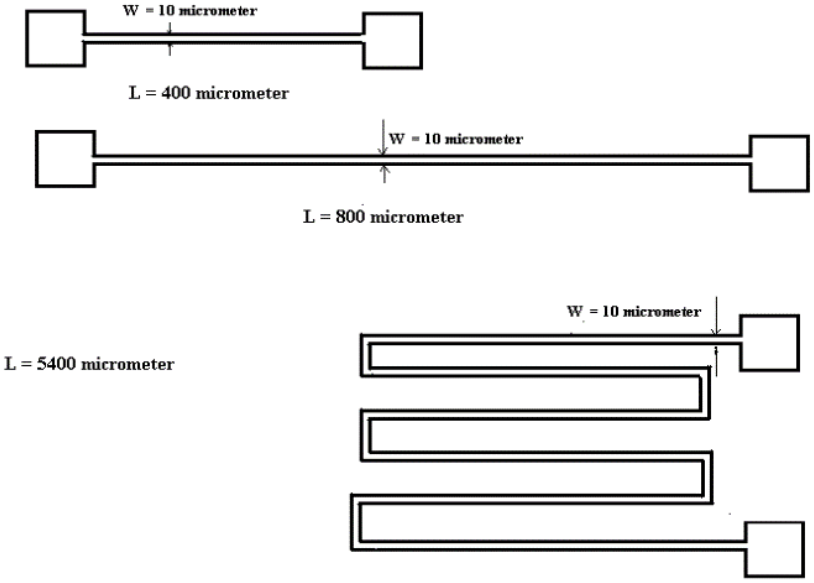

Figure 3.5: *IC resistor L=10, 400, 5400μm*

Three types of Resistors, which are shown in Figure 3.5, represented as R400, R800 and R5400.

$$R = R_{sh} \cdot (\frac{L}{W})_{eff} \tag{3.7}$$

Here for making the pad corrections in R400, R800 and R5400, we just add 40 micrometers to the nominal lengths to have 440, 840, and 5440 micrometers accordingly. In the R5400 we need to make the correction for bends.

3.2 PN Diode Measurements

3.2.1 Fundamental Structure Concepts

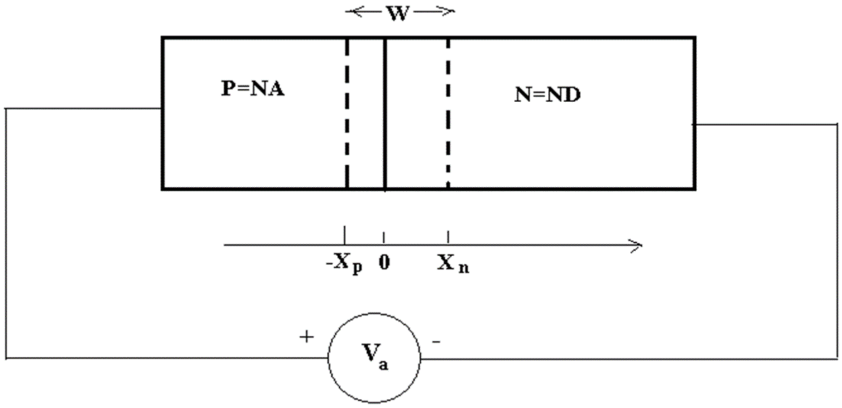

Figure 3.6: *Cross Section of PN Diode*

Figure 3.6 shows the cross section of a PN diode.
where
W is the width of depletion region (cm).
x_n is the width of depletion region in n-type part (cm).
x_p is the width of depletion region in p-type part (cm).
N_A is the doping concentration of acceptor (cm^{-3}).
N_D is the doping concentration of donor (cm^{-3}).
V_a is the externally applied voltage source (V).

The built potential is given as:

$$V_{bi} = \frac{kT}{q} \cdot ln(\frac{N_n \cdot P_p}{n_i^2}) \tag{3.8}$$

where
V_{bi} is the built-in potential (V).
k is the Boltzmann constant, which is about 8.617x10^{-5} (eV/K).
T is the room temperature, which is about 300 (K).
q is the elementary charge, which is about 1.6x10^{-19} (C)
n_i is the intrinsic carrier concentration of Si at 300K, which is about 1.5x10^{10} (cm^{-3})

Using the above assumptions, following a lengthy derivation we can derive the following equation which describes the current-voltage ($I - V$) characteristics of a PN diode:

$$I = I_0 \cdot (e^{\frac{qV}{nkT}} - 1) \tag{3.9}$$

where
I is the measured current (A)

I_0 is the reverse saturation current, which is usually in (pA) level.
n is a correction factor which takes into account all non-ideal effects and is called ideality factor and in most cases it is usually between 1 and 2.

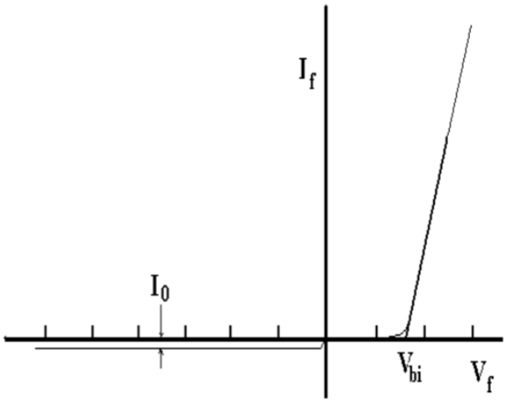

Figure 3.7: *I vs. V_r in PN Diode*

Values of n, I_0 and V_{bi} are experimentally extracted from the DC data.

3.2.2 $I - V$ Characteristic Curve

In the diode $I - V$ formula, for all practical purposes in the forward bias regime, we can rewrite the equation as:

$$I = I_0 \cdot (e^{\frac{qV}{nkT}}) \tag{3.10}$$

Taking the natural logarithm of the above relation results in a linear relation for $ln(I)$ vs. V:

$$ln(I) = ln(I_0) + \frac{qV}{nkT} \tag{3.11}$$

Figure 3.8 shows the theoretical and experimental Graph of $ln(I)$ vs V_r.

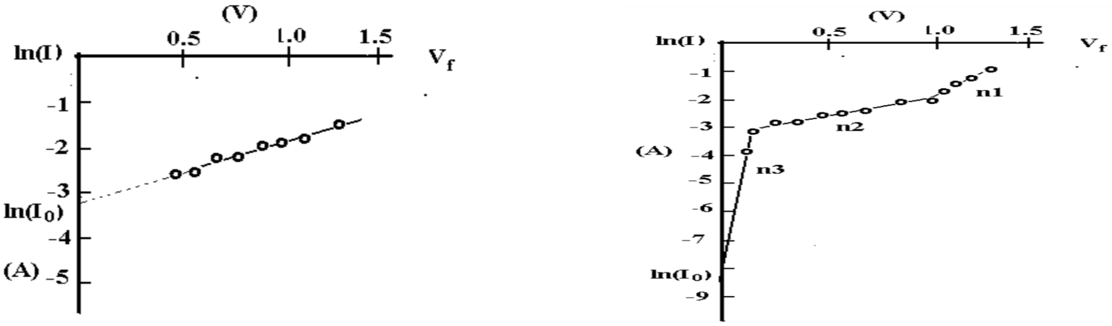

Figure 3.8: *Theoretical and Experimental Graph of $ln(I)$ vs V_r*

3.3 MOS Capacitor Measurements

3.3.1 Fundamental Structure Concepts

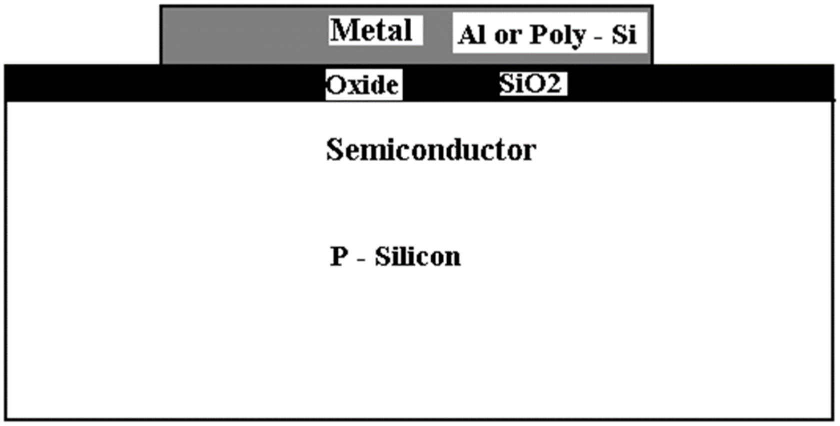

Figure 3.9: *Cross Section of MOS Capacitor*

Figure 3.9 shows the cross section of a MOS capacitor.

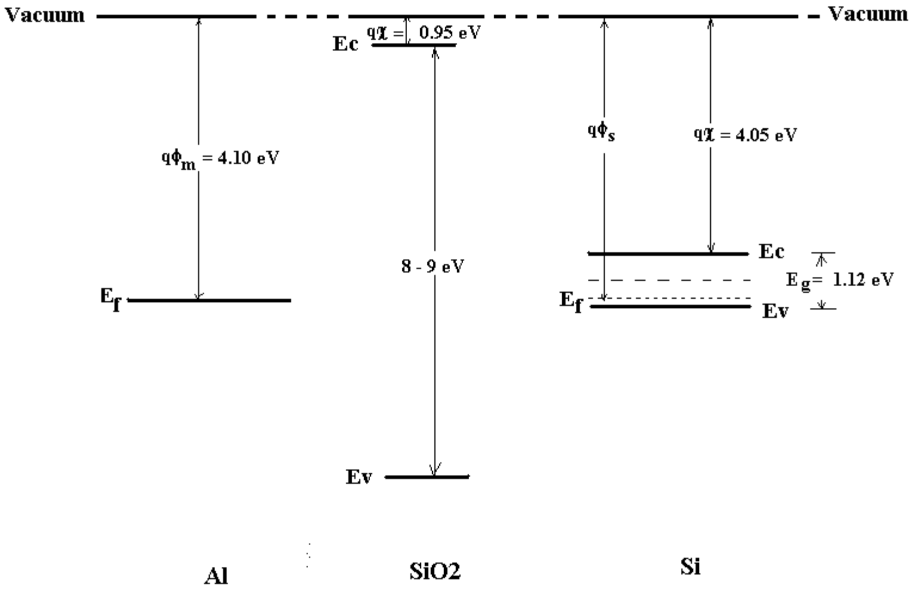

Figure 3.10: *Band structure of MOS capacitor*

Figure 3.10 shows the band structures. Figure 3.11 shows four cases when different external voltage is applied. For (*a*), it is the flat band situation, for (*b*), it's in accumulation regime, for (*c*), it's in depletion regime and for (*d*), it's in inversion regime.

Figure 3.12 shows the $C - V$ relationship.

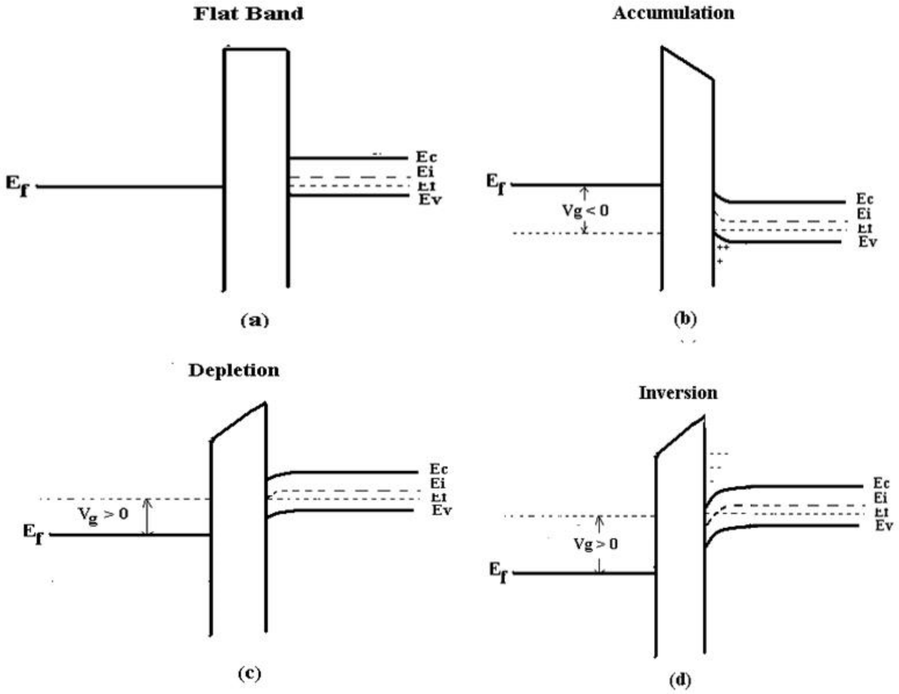

Figure 3.11: *Band structure at different conditions*

3.3.2 Extraction of Oxide Thickness from the $C - V$ Data

The extraction of oxide thickness from the $C - V$ data is:

$$C_{SiO_2} = \frac{\epsilon_{ox}\epsilon_0 A}{t_{ox}} \tag{3.12}$$

where
C_{SiO_2} is the capacitance of SiO$_2$ (F).
ϵ_{ox} is the oxide (SiO$_2$) relative permittivity, which is about 3.9.
ϵ_0 is the permittivity of the free space, which is about 8.85x10^{-14} (F/cm).
A is the area of the capacitor. (cm^2).
t_{ox} is the oxide thickness (cm).

And also

$$\begin{aligned} C_{Si} &= \frac{\epsilon_{Si}\epsilon_0 A}{W} \\ C_{sf} &= \frac{C_{Si} \cdot C_{SiO_2}}{C_{Si} + C_{SiO_2}} \end{aligned} \tag{3.13}$$

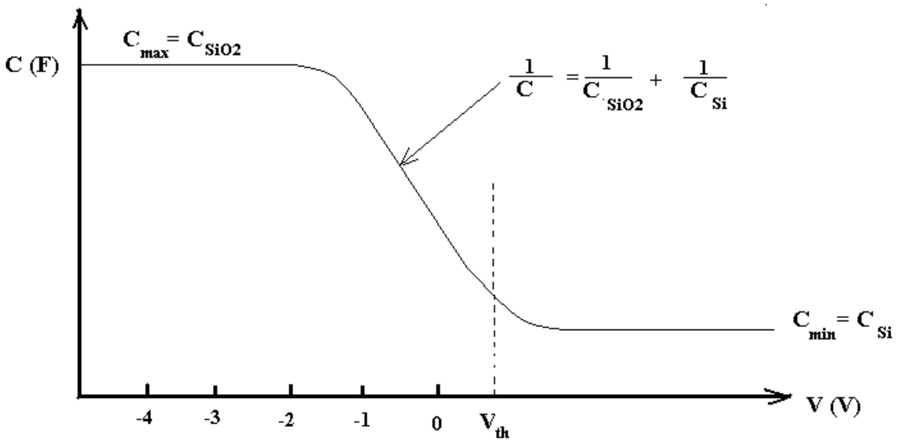

Figure 3.12: *MOS Capacitors $C - V$ Characteristics*

3.3.3 Extraction of N_{sub}

After extraction of N_{sub}:

$$\begin{aligned} \phi_f &= \frac{kT}{q} \cdot ln(\frac{N_A}{n_i}) > 0 \qquad p - type semiconductor(V) \\ \phi_f &= \frac{kT}{q} \cdot ln(\frac{n_i}{N_D}) < 0 \qquad n - type semiconductor(V) \\ N_{sub} &= \frac{4\phi_f C_{sf}^2}{q\epsilon_{Si}\epsilon 0 A^2} \end{aligned} \tag{3.14}$$

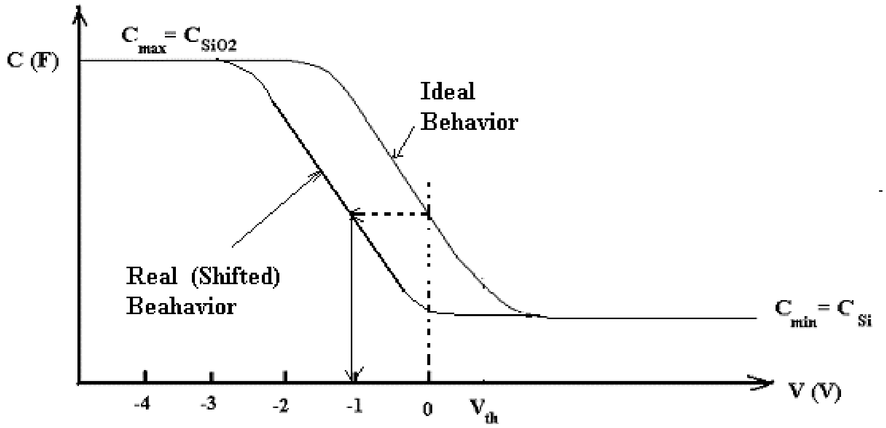

Figure 3.13: *$C - V$ Shift Due to Oxide Charges and Metal-Semiconductor Work Function Differences*

3.3.4 Extraction of Oxide Charges

The extraction of oxide charges:

$$C_{FB} = \phi_{MS} + \frac{Q_{ss}}{C_{SiO_2}} \tag{3.15}$$

where
Φ_{MS}=Φ_M-Φ_S
Φ_m is the metal work function, which is about 4.10 (eV) for Aluminum.
Φ_s is the semiconductor work function in (eV), which is equal to $\chi_{Si} + \frac{E_g}{2} + \phi_f$.
where
χ is the electron affinity (V).
E_g is the band gap of silicon at 300 (K), which is about 1.12 (eV).

The flat band capacitance is:

$$C_{FB} = \frac{1}{\frac{1}{C_{OX}} + \frac{L_d}{\epsilon_{Si}\epsilon_0 A}} \tag{3.16}$$

where
L_d is the Deby length, which is equal to $L_d = \sqrt{\frac{\epsilon_{Si}\epsilon_0 kT}{q^2 N_A}}$.

The number of charges per unit area of the capacitor (N_f) can be found by:

$$N_f = Q_{ss}/(q \cdot Area\ of\ the\ capacitor) \tag{3.17}$$

3.4 MOSFET Measurements

3.4.1 Fundamental Structure Concepts

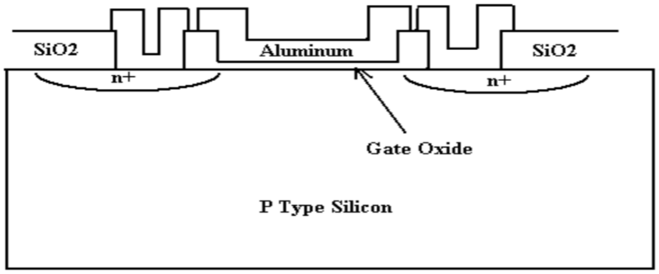

Figure 3.14: *Cross Section of MOSFET*

Figure 3.14 shows the cross section of a MOSFET.
And here are some assumptions used for MOSFET square law model:

- We assume that we have long channel (L>5 μm).
- We assume the mobility of electrons is constant in the channel.
- We assume that shape of the channel (same as the MOS inversion layer) as a function of the drain-source bias changes linearly (gradualchannel approximation, GCA).
- We assume that electric along the channel is the dominant electric field and the component of electric perpendicular to the channel inside the semiconductor is negligible. For long channel MOSFET, this is a fairly good approximation.

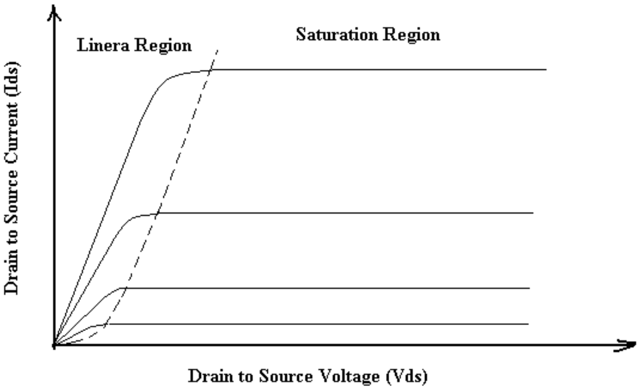

Figure 3.15: *$I-V$ Characteristics of MOSFET[2]*

Figure 3.15 shows the $I-V$ characteristic curve of MOSFET.

3.4.2 Linear Regime

The $I - V$ characteristic in linear regime is:

$$I_{ds} = \frac{\bar{\mu} C_0 W}{L} \cdot [(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}] \tag{3.18}$$

where
I_{ds} is the drain-to-source current (A).
$\bar{\mu}$ is the average mobility of carriers in the channel $(cm^2/(V \cdot s))$.
C_0 is the capacitance per area of the MOS structure (F/cm^2).
W is the MOSFET width (μm).
L is the MOSFET gate length (μm).
V_{gs} is the gate-to=source voltage (V).
V_{th} is the threshold voltage (V).
V_{ds} is the drain-to-source voltage (V).

3.4.3 Linear-Saturation Transition

The above relationship represent the "linear regime" of the MOSFET $I - V$ characteristic, which is shown in Figure 3.15.

In the regime of $V_{ds} > V_{ds,sat}$, where $V_{ds,sat}$ represent the drain-to-source voltage, beyond which any increase in the value of V_{ds} would not bring about any further increase in the I_{ds}. This regime is called saturation regime.

3.4.4 Saturation Regime

Saturation regime is the most important part of transistors operating regime where a flat characteristics (at least theoretically) allows the circuit designers use the transistors over a wide operating voltages. Therefore, most of our device parameter extraction is done in the saturation regime.

In order to find $V_{ds,sat}$, we realize that the onset of the saturation is where the relationship defined as square law model has a maximum I_{ds}, therefore in order to find $V_{ds} = V_{ds,sat}$, all we need to do is to differentiate Ids with respect to V_{ds} and solve for V_{ds}. We then find:

$$V_{ds} = V_{ds,sat} = V_{gs} - V_{th} \tag{3.19}$$

Replacing V_{ds} in the square law formula above, we can find an expression for $V_{ds,sat}$ as:

$$I_{ds,sat} = \frac{\bar{\mu} C_0 W}{2L} \cdot (V_{gs} - V_{th})^2 \tag{3.20}$$

As this expression indicates, The saturation current ($I_{ds,sat}$) of a MOSFET is only a function of varying $V_g s$ and not a function of $V_d s$.

3.4.5 Extraction of Threshold Voltage & Average Channel Mobility in Saturation Regime

Taking square root of the previous $I - V$ relationship, we have:

$$\sqrt{I_{ds,sat}} = \sqrt{\frac{\bar{\mu} C_0 W}{2L}} \cdot (V_{gs} - V_{th}) \tag{3.21}$$

And the curve is shown as below:

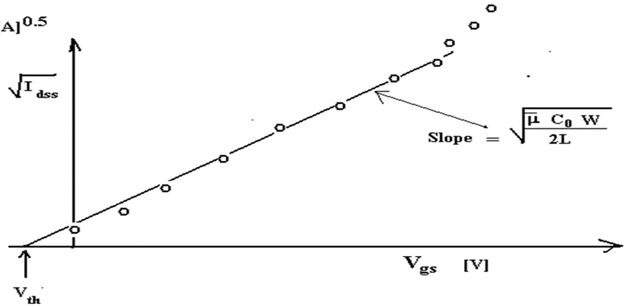

Figure 3.16: *Graph of* $\sqrt{I_{ds,sat}}$ *vs* V_{gs} *of MOSFET*

The value of V_{th} and $\bar{\mu}$ can be found in Figure 3.16.

3.4.6 Extraction of Saturation Velocity

There is also another way of looking at the saturation regime, and that is to attribute the saturation of the drain current to the carriers in the channel have reached their saturation velocity (V_S).

Modifying the square law model to implement V_S in this equation, we need to replace V_S with:

$$V_S = \frac{\mu(V_{gs} - V_{th})}{2L} \tag{3.22}$$

And we can rewrite the square law model as:

$$I_{ds,sat} = V_S C_0 W (V_{gs} - V_{th}) \tag{3.23}$$

Now if we plot $I_{ds,sat}$ as a function of Vs we expect an almost linear relationship, which would enable us to extract V_S from the slope of this graph at higher V_{gs} values only:

The saturation velocity can be calculated from Figure 3.17.

3.4.7 Extraction of Transconductance

The most important figure of merit of MOSFET is transconductance (g_m) which represents the conductance (inverse of the resistance) of the channel and is defined as:

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} \qquad at\ V_{ds} = cte \tag{3.24}$$

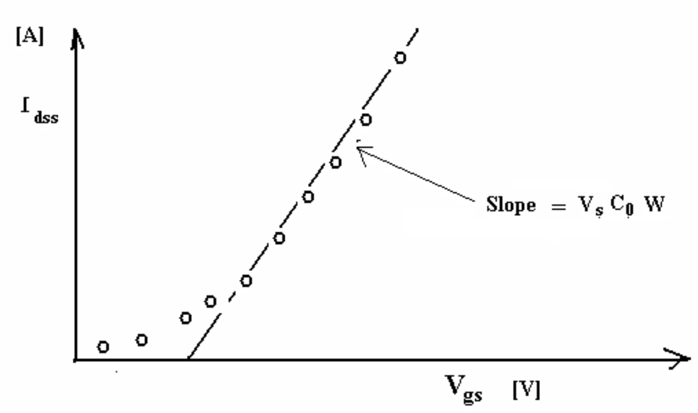

Figure 3.17: *Graph of $I_{ds,sat}$ vs V_{gs} of MOSFET*

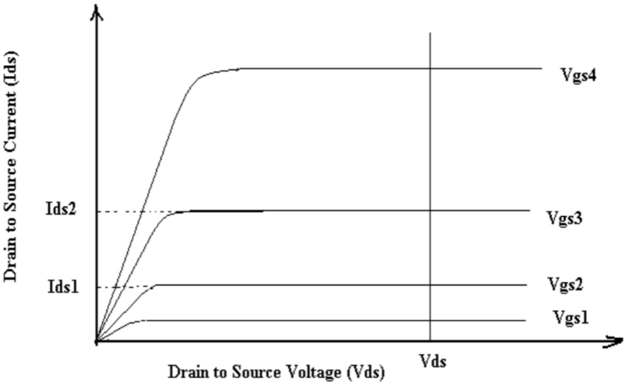

Figure 3.18: *Graph of g_m vs V_{gs} of MOSFET in Saturation Regime*

We are usually interested in the transconductance for the saturation regime, therefore, we approximate $\frac{\delta I_{ds}}{\delta V_{gs}}$ with $\frac{\Delta I_{ds}}{\Delta V_{gs}}$, where $\frac{\Delta I_{ds}}{\Delta V_{gs}} = \frac{I_{ds,2}-I_{ds,1}}{V_{gs,2}-V_{gs,1}}$.

Figure 3.18 shows the graph of g_m vs V_{gs} in saturation regime.

3.4.8 Extraction of Output Conductance

The second most important figure of merit for DC characterization of a Field Effect Transistor is output conductance, g_d which is defined as:

$$\begin{aligned} g_d &= \frac{\delta I_{ds}}{\delta V_{ds}} \\ g_d &\approx \frac{\Delta I_{ds}}{\Delta V_{ds}} \qquad at\ V_{gs} = cte \\ g_d &\approx \frac{I_{ds,2} - I_{ds,1}}{V_{ds_2} V_{ds,1}} \end{aligned} \tag{3.25}$$

Figure 3.20 shows the graph of g_d vs V_{ds} in saturation regime.

Figure 3.21 shows the graph of g_d vs V_{gs} in saturation regime.

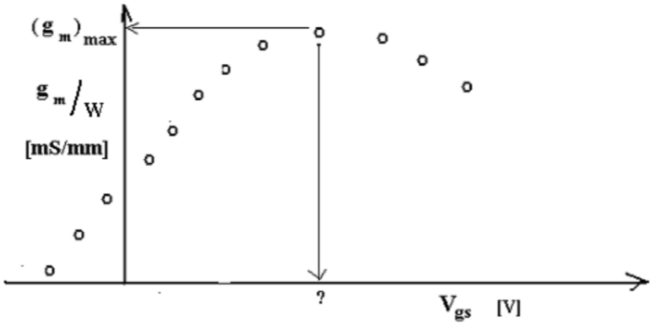

Figure 3.19: *Graph of g_m vs V_{gs} & Extraction of $g_{m,max}$ & the Corresponding V_{gs}*

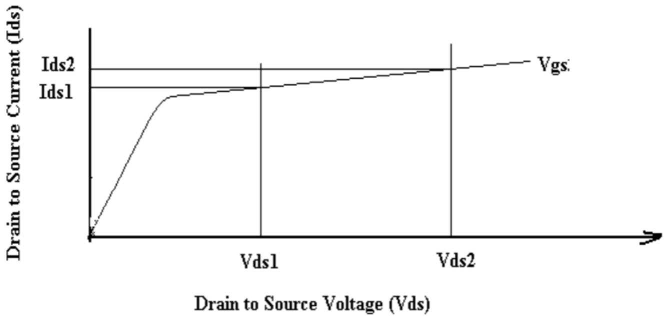

Figure 3.20: *Graph of g_d vs V_{ds} in Saturation Regime*

3.4.9 Voltage Swing

Figure 3.22 shows the graph of voltage swing, which represents the V_{gs} corresponding to $(\frac{g_m}{g_d})_{max} - 10\%(\frac{g_m}{g_d})_{max}$.

3.4.10 Channel Conductance and Extraction of Mobility in Linear Regime

The channel conductance is defined as:

$$\begin{aligned} g_c &= \frac{\delta I_{ds}}{\delta V_{ds}} \qquad\qquad at\ V_{gs} = cte \\ &= \frac{\bar{\mu} C_0 W}{L} \cdot [(V_{gs} - V_{th}) - V_{ds}] \end{aligned} \tag{3.26}$$

In the linear regime, since V_{ds} values are very small (i.e. $V_{ds} < 0.2V$), and therefore we can approximate the above as:

$$\begin{aligned} g_c &= \frac{\bar{\mu} C_0 W}{L} \cdot (V_{gs} - V_{th}) \\ g_c &\approx \frac{\Delta I_{ds}}{\Delta V_{ds}} \qquad\qquad at\ V_{gs} = cte \\ g_c &\approx \frac{I_{ds,2} - I_{ds,1}}{V_{ds_2} V_{ds,1}} \end{aligned} \tag{3.27}$$

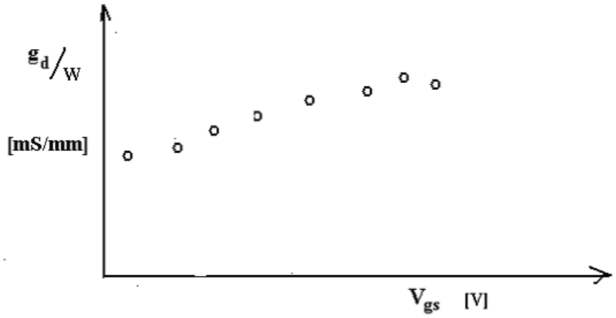

Figure 3.21: *Graph of g_d vs V_{gs} in Saturation Regime*

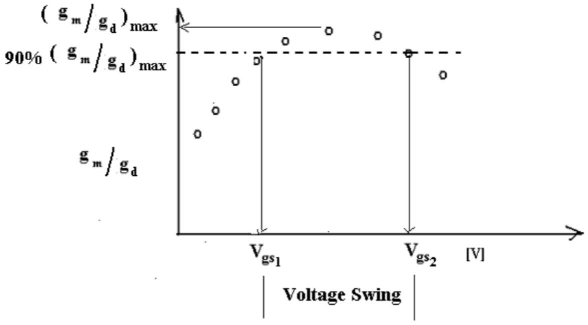

Figure 3.22: *Graph of Voltage Swing*

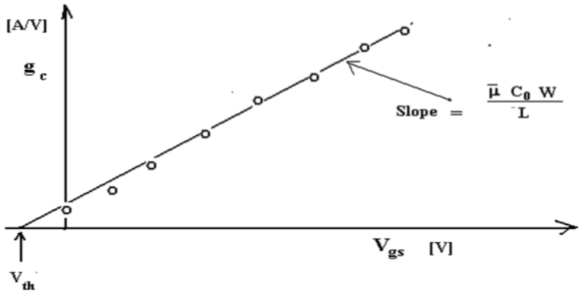

Figure 3.23: *Graph of g_c vs V_{gs} in Linear Regime*

Figure 3.23 shows the g_c vs V_{gs} graph in linear regime.

4. Result

4.1 Resistor Measurements

4.1.1 Sheet Resistor Measurement

Three resistors with different lengths of 400 μm, 800 μm and 5400 μm are measured. The effective square number (N) for these resistors are:

$$\begin{aligned} N_{sh,400} &= 440/10 = 44 \\ N_{sh,800} &= 840/10 = 84 \\ N_{sh,5400} &= 5440/10 - 17 \times 0.44 = 536.52 \end{aligned} \tag{4.1}$$

The data and the calculation result are shown in Table 4.1.

Table 4.1: *Sheet Resistance Measurements*

L (μm)	400	800	5400
W (μm)	10	10	10
U (V)	0.5	0.5	0.5
I (mA)	1.988	1.016	0.181
$R_{measured}$ (Ω)	251.509	492.126	2762.431
N (μm)	44	84	536.52
R_{sh} ($\Omega/\Box$)	5.716	5.859	5.147
$R_{sh,avg}$ ($\Omega/\Box$)		5.574	

4.1.2 Transfer Line Method

Table 4.2 shows the resistance of the transfer line.

Figure 4.1 shows the resistance vs distance relationship for TSM20. The linear function is:

$$y = 0.2151x + 9.602 \tag{4.2}$$

The R^2 fitting value is pretty high, which means the linearity of the curve is good. The slope of it is 0.2151 ($\Omega/\mu m$) and the intercept is 9.602 (Ω).

Table 4.2: *Transfer Line Resistance Measurements*

Pad Section	**Distance** (μm)	U (V)	$I(mA)$	**Resistance** (Ω)
4-5	60	0.5	22.59	22.13
5-6	100	0.5	15.97	31.31
6-7	200	0.5	9.47	52.80
7-8	300	0.5	6.71	74.56
8-9	380	0.5	5.50	90.93

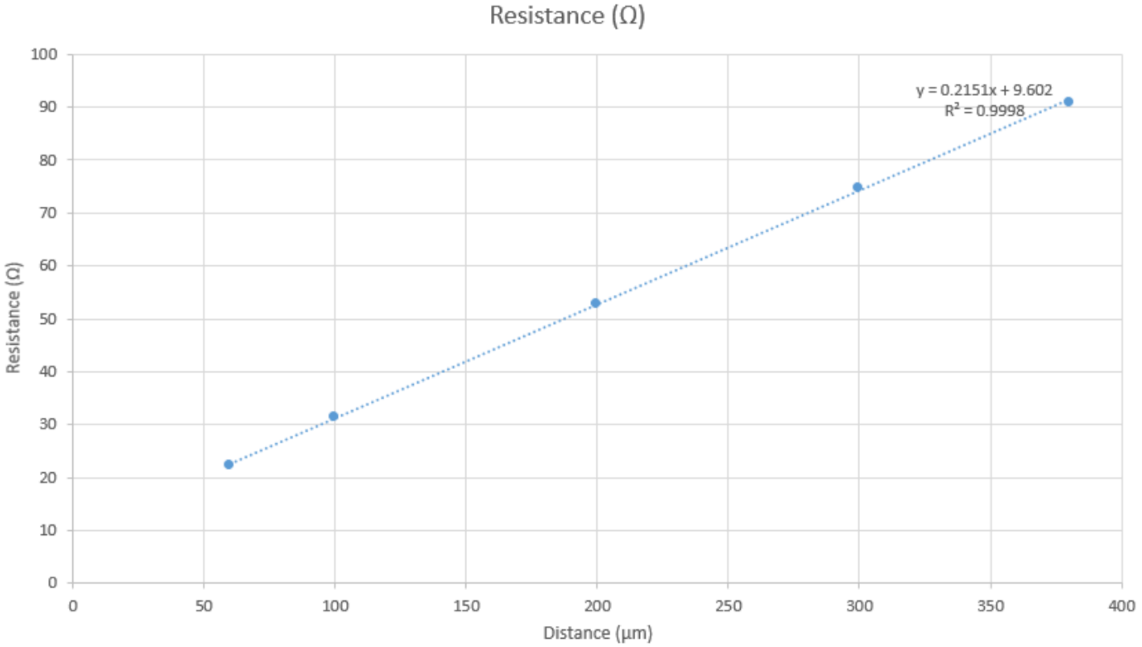

Figure 4.1: *R (Ω) vs d (µm) Relationship for TLM20*

Then we can calculate the R_C and R_{sh} values as:

$$\begin{aligned} R_C &= 9.602/2 = 4.801\ (\Omega) \\ Slope &= R_{sh}/Z = 0.2151\ (\Omega/\mu m) \\ R_{sh} &= 0.2151 \times 20 = 4.302\ (\Omega/\square) \end{aligned} \tag{4.3}$$

4.2 PN Diode Measurements

4.2.1 Built-in Voltage Measurement

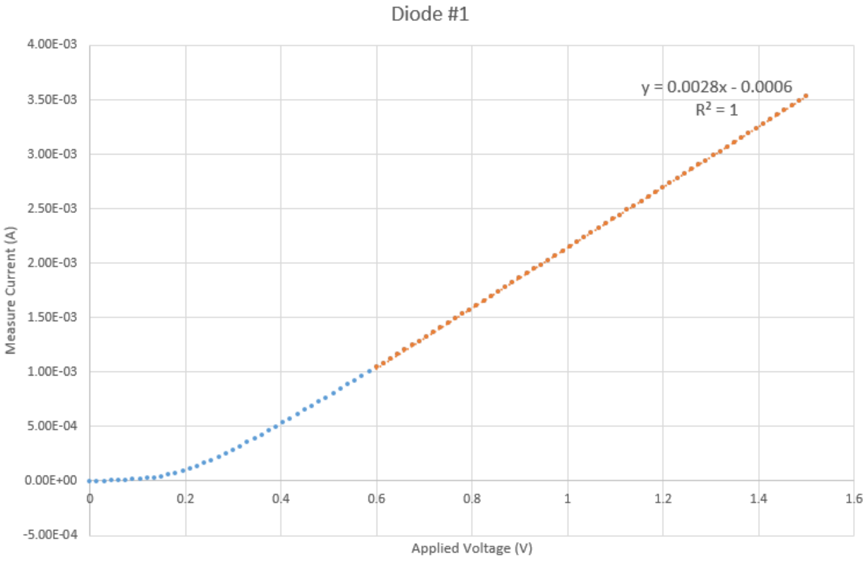

Figure 4.2: *Measured Current I (A) vs Applied Voltage V (V) for Diode #1*

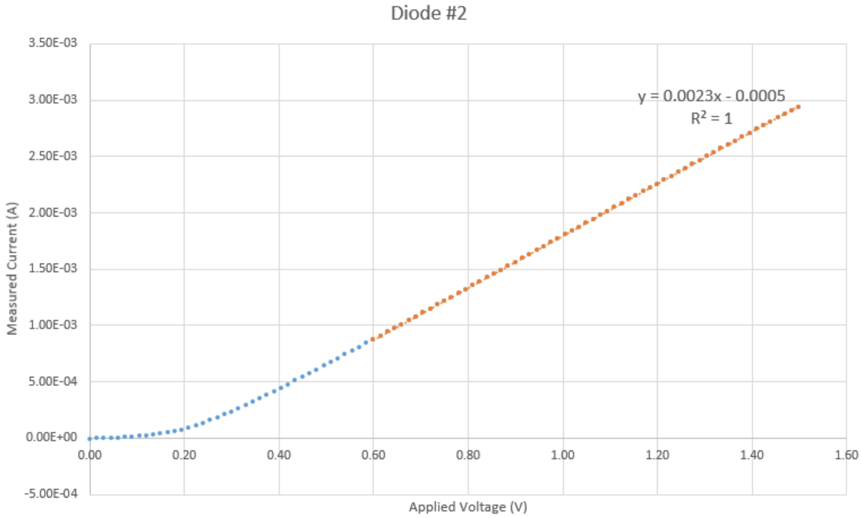

Figure 4.3: *Measured Current I (A) vs Applied Voltage V (V) for Diode #2*

Figure 4.2 and 4.3 shows the measured current and applied voltage relationship for both two PN diodes.The two linear functions can be used to approximately calculate the built-in potential V_{bi}.

Table 4.3 shows the calculated results, the built-in potential is 0.214 (V) for diode #1 and 0.217 (V) for diode #2.

Table 4.3: *Built-in Potential V_{bi} Calculation*

	Diode #1	Diode #2
Equation	y=0.0028x-0.0006	y=0.0023x-0.0005
V_{bi} (V)	0.214	0.217

4.2.2 Ideality Factor Measurement

After transforming the current to the natural logarithm value, we can get Figure 4.4 and 4.5.

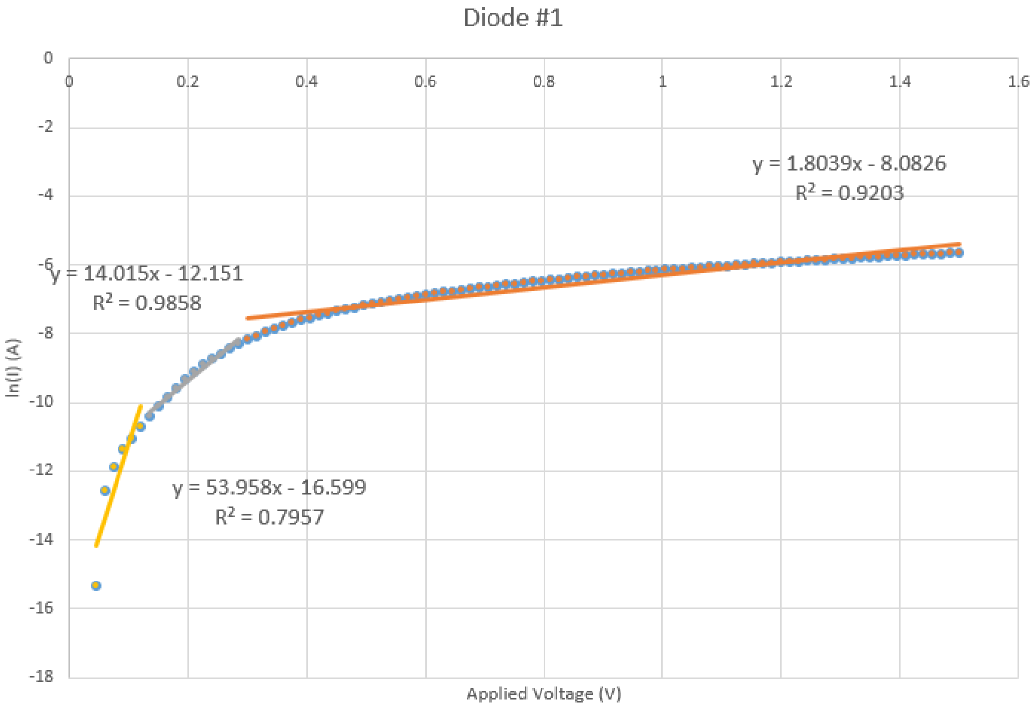

Figure 4.4: *Measured Current ln(I) (A) vs Applied Voltage V (V) for Diode #1*

For each curve in Figure 4.4 and 4.5, we can divide it into three parts, and for each part, it can fitted by a linear function. For each linear function, we can get a pair of ideality factor n and reverse saturation current I_0 based on the equation:

$$ln(I) = ln(I_0) + \frac{qV}{nkT} \tag{4.4}$$

We can have the solution that:

$$\begin{gathered} slope = \frac{q}{nkT} \\ n = \frac{q}{kT} \times \frac{1}{slope} \\ ln(I_0)\ is\ the\ intercept\ of\ y\ axis. \end{gathered} \tag{4.5}$$

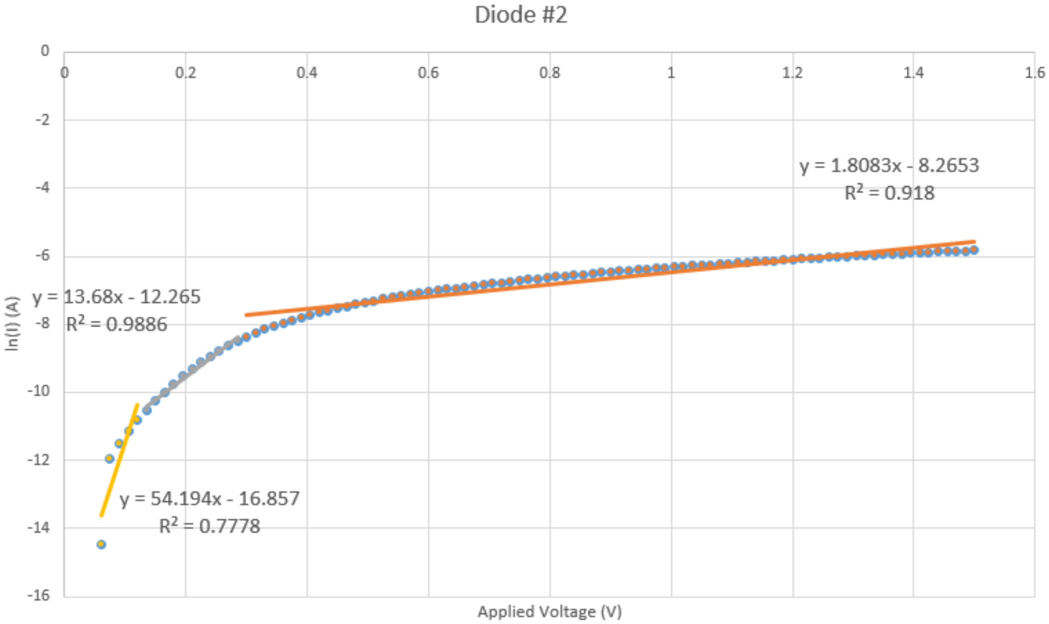

Figure 4.5: *Measured Current ln(I) (A) vs Applied Voltage V (V) for Diode #2*

Table 4.4: *Ideality Factor n & Reverse Saturation Current I_0 Calculation*

	n_1	n_2	n_3	$ln(I_0)$ (A)	I_0 (nA)
Diode #1	0.717	2.760	21.443	-16.599	61.82
Diode #2	0.714	2.828	21.391	-16.857	47.77

Table 4.4 shows the ideality factor n and reverse saturation current I_0. For two diodes, the ideality factors are similar, and for reverse currrnt, they are both in (nA) level, which make sense.

4.3 MOS Capacitor Measurements

4.3.1 MOS Capacitor C-V Characteristics Measurement

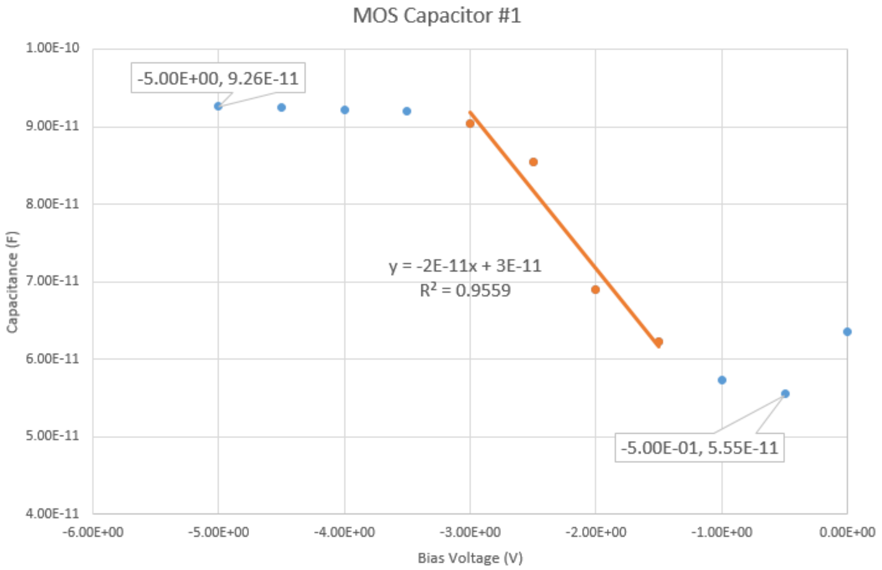

Figure 4.6: *Capacitance C (F) vs Bias Voltage V (V) for MOS Capacitor #1*

The MOS capacitor $C - V$ characteristics are shown in Figure 4.6 and 4.7. Based on the curves, we can calculate the value oxide capacitance C_{SiO_2}, silicon capacitance C_{Si} and the series capacitance C_{sf} based on the equations below:

$$\begin{aligned} C_{SiO_2} &= C_{max} \\ C_{Si} &= C_{min} \\ C_{sf} &= \frac{C_{Si} \cdot C_{SiO_2}}{C_{Si} + C_{SiO_2}} \end{aligned} \tag{4.6}$$

Table 4.5 shows the value oxide capacitance C_{SiO_2}, silicon capacitance C_{Si} and the series capacitance C_{sf} C_{Si} for both two MOS capacitors.

Table 4.5: *Oxide Capacitance C_{SiO_2} & Silicon Capacitance C_{Si} Calculation*

	C_{SiO_2} (pF)	C_{Si} (pF)	C_{sf} (pF)
MOS Capacitor #1	92.6	55.5	34.7
MOS Capacitor #2	98.8	57.7	36.4

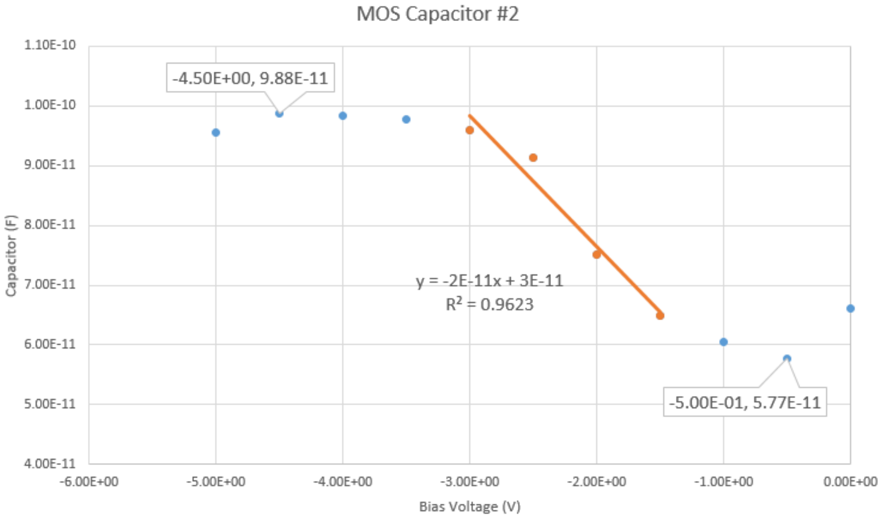

Figure 4.7: *Capacitance C (F) vs Bias Voltage V (V) for MOS Capacitor #2*

4.3.2 Extraction of Oxide Thickness from C-V Data

Since we already have the value of C_{SiO_2}, we can derive the value of the thickness the oxide layer t_{ox} based on the equation:

$$\begin{aligned} C_{SiO_2} &= \frac{\epsilon_{ox}\epsilon_0 A}{t_{ox}} \\ t_{ox} &= \frac{\epsilon_{ox}\epsilon_0 A}{C_{SiO_2}} \end{aligned} \tag{4.7}$$

where
ϵ_{ox} is the oxide (SiO_2) relative permittivity, which is about 3.9.
ϵ_0 is the permittivity of the free space, which is about 8.85x10^{-14} (F/cm).
A is the area of the capacitor, here since it's a square, so its value is 1.6×10^{-3} (cm^2).

Then for both MOS capacitors #1 and #2, we can have the value of t_{ox}:

$$\begin{aligned} t_{ox,1} &= \frac{3.9 \times 8.85 \times 10^{-12} \times 1.6 \times 10^{-3}}{92.6 \times 10^{-12}} = 5.964 \times 10^{-6}\ (cm) = 596.4\ (A) \\ t_{ox,2} &= \frac{3.9 \times 8.85 \times 10^{-12} \times 1.6 \times 10^{-3}}{98.8 \times 10^{-12}} = 5.589 \times 10^{-6}\ (cm) = 558.9\ (A) \end{aligned} \tag{4.8}$$

4.3.3 Extraction of N_{sub}

For the value of N_{sub} and N_A, we can apply iteration function to based on the equations:

$$\begin{aligned} N_{sub} &= \frac{4\phi_f C_{sf}^2}{q \times \epsilon_{Si} \times \epsilon_0 \times A^2} \\ N_{sub} &= N_A \\ \phi_f &= \frac{kT}{q} \times ln(\frac{N_A}{n_i}) \qquad For\ p-type\ wafer \end{aligned} \tag{4.9}$$

where

ϵ_{Si} is the relative permittivity of silicon, whose value is about 11.68.

For MOS capacitor #1, the iteration sequence is as in Table 4.6:

Table 4.6: *Iteration for MOS Capacitor #1*

N_A (cm^{-3})	N_{sub} (cm^{-3})
1.00×10^{15}	3.26×10^{15}
3.26×10^{15}	3.61×10^{15}
3.61×10^{15}	3.64×10^{15}
3.64×10^{15}	3.64×10^{15}

The value of N_{sub} is 3.64×10^{15} (cm^{-3}) and ϕ_f is 0.321 (V).

For MOS capacitor #2, the iteration sequence is as in Table 4.7:

Table 4.7: *Iteration for MOS Capacitor #2*

N_A (cm^{-3})	N_{sub} (cm^{-3})
1.00×10^{15}	3.59×10^{15}
3.59×10^{15}	4.00×10^{15}
4.00×10^{15}	4.04×10^{15}
4.04×10^{15}	4.04×10^{15}

The value of N_{sub} is 4.04×10^{15} (cm^{-3}) and ϕ_f is 0.323 (V).

4.3.4 Extraction of Oxide Charge

For the oxide charge, we should firstly calculate the Deby length L_d, for both MOS Capacitors #1 and #2,

$$\begin{aligned} L_{d,1} &= \sqrt{\frac{\epsilon_{Si}\epsilon_0 kT}{q^2 N_{A,1}}} = 6.769\times10^{-6}\ (cm) \\ L_{d,2} &= \sqrt{\frac{\epsilon_{Si}\epsilon_0 kT}{q^2 N_{A,2}}} = 6.425\times10^{-6}\ (cm) \end{aligned} \tag{4.10}$$

Then we can calculate the value of flat-band capacitance C_{FB}, which are:

$$\begin{aligned} C_{FB,1} &= \frac{1}{\frac{1}{C_{OX}} + \frac{L_{d,1}}{\epsilon_{Si}\epsilon_0 A}} = 67.2\ (pF) \\ C_{FB,2} &= \frac{1}{\frac{1}{C_{OX}} + \frac{L_{d,2}}{\epsilon_{Si}\epsilon_0 A}} = 71.4\ (pF) \end{aligned} \tag{4.11}$$

Based on the linear fitting equation in Figure 4.6 and 4.7, we can calculate the values of

V_{FB} for both MOS capacitors #1 and #2:

$$\begin{aligned}
y_1 &= -2 \times 10^{-11} \times x_1 + 3 \times 10^{-11} \\
C_{FB,1} &= -2 \times 10^{-11} \times V_{FB,1} + 3 \times 10^{-11} \\
\Rightarrow \qquad V_{FB,1} &= -1.86\ (V) \\
y_2 &= -2 \times 10^{-11} \times x_2 + 3 \times 10^{-11} \\
C_{FB,2} &= -2 \times 10^{-11} \times V_{FB,2} + 3 \times 10^{-11} \\
\Rightarrow \qquad V_{FB,2} &= -2.07\ (V)
\end{aligned} \tag{4.12}$$

Then for the work functions, we can calculate them for both metal and silicon based on equations below:

$$\begin{aligned}
\phi_{S,1} &= \chi_{Si} + \frac{E_g}{2} + \phi_{f,1} = 4.05 + \frac{1.12}{2} + 0.321 = 4.931\ (V) \\
\phi_{MS,1} &= \phi_M - \phi_{S,1} = 4.10 - 4.931 = -0.831\ (V) \\
\phi_{S,2} &= \chi_{Si} + \frac{E_g}{2} + \phi_{f,2} = 4.05 + \frac{1.12}{2} + 0.323 = 4.933\ (V) \\
\phi_{MS,2} &= \phi_M - \phi_{S,2} = 4.10 - 4.931 = -0.833\ (V)
\end{aligned} \tag{4.13}$$

The charges on the surface can be calculated as:

$$\begin{aligned}
Q_{ss,1} &= (V_{FB,1} - \phi_{MS,1}) \times C_{SiO_2,1} \\
&= [-1.86 - (-0.831)] \times 92.6 \times 10^{-12} = -9.529 \times 10^{-11}\ (C) \\
Q_{ss,2} &= (V_{FB,2} - \phi_{MS,2}) \times C_{SiO_2,2} \\
&= [-2.07 - (-0.833)] \times 98.8 \times 10^{-12} = -1.222 \times 10^{-10}\ (C)
\end{aligned} \tag{4.14}$$

Therefore, the value of oxide charge can be derived as:

$$\begin{aligned}
N_{f,1} &= \frac{Q_{ss,1}}{q \times A} = \frac{-9.529 \times 10^{-11}}{-1.60 \times 10^{-16} \times 1.60 \times 10^{-3}} = 3.722 \times 10^{11}\ (cm^{-2}) \\
N_{f,2} &= \frac{Q_{ss,2}}{q \times A} = \frac{-1.222 \times 10^{-10}}{-1.60 \times 10^{-16} \times 1.60 \times 10^{-3}} = 4.773 \times 10^{11}\ (cm^{-2})
\end{aligned} \tag{4.15}$$

4.4 MOSFET Measurements

4.4.1 I-V Characteristic Curve

The $I_{ds} - V_{ds}$ characteristics curves of MOSFET are shown below, which include $L = 16\mu m$, $W = 40\mu m$ MOSFET and $L = 16\mu m$, $W = 80\mu m$ MOSFET in both linear and saturation regimes.

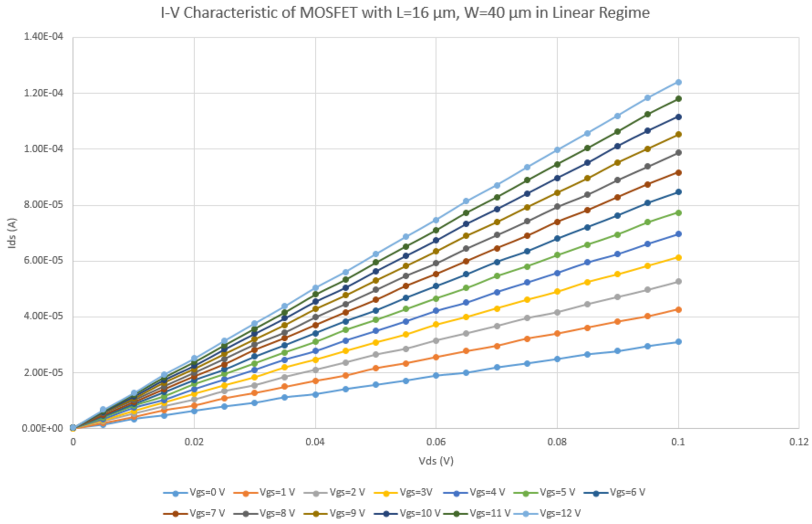

Figure 4.8: *I-V Curve of MOSFET with L=16 µm, W=40 µm in Linear Regime*

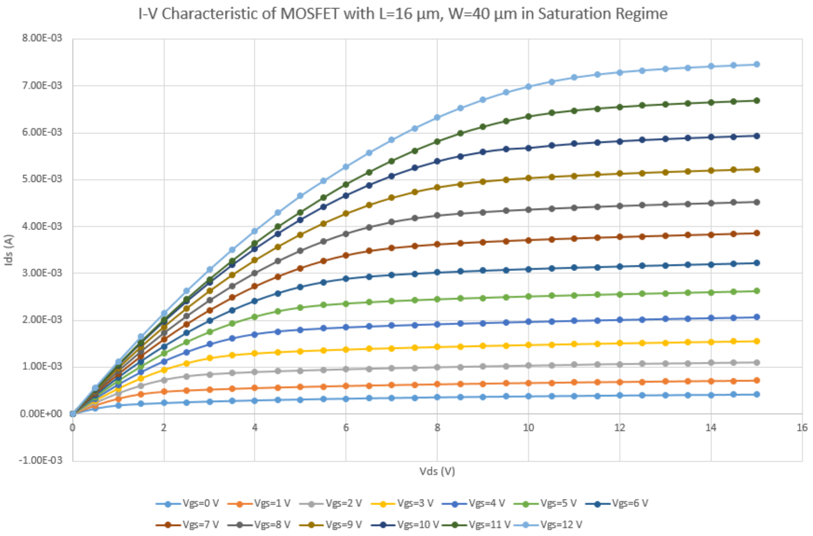

Figure 4.9: *I-V Curve of MOSFET with L=16 µm, W=40 µm in Saturation Regime*

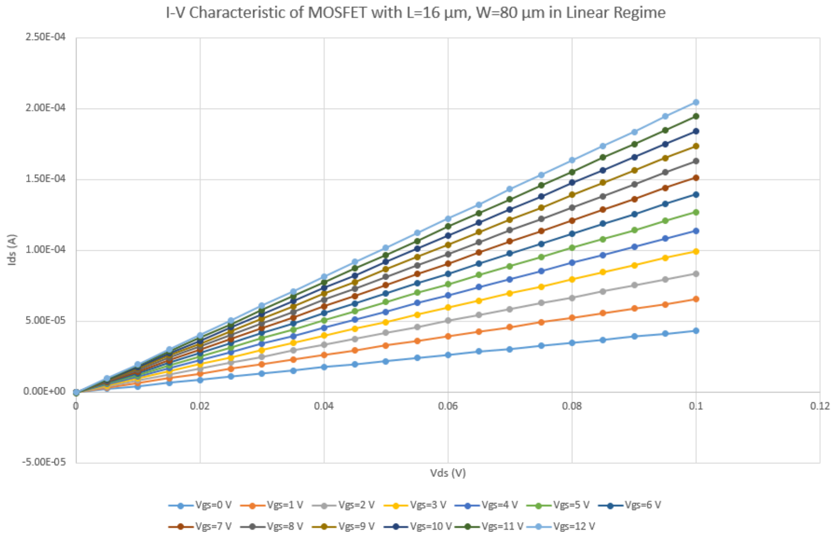

Figure 4.10: *I-V Curve of MOSFET with L=16 µm, W=80 µm in Linear Regime*

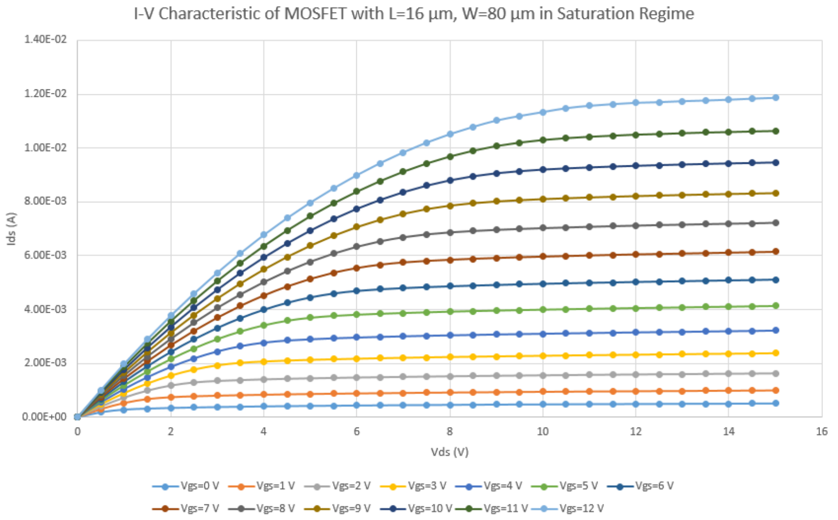

Figure 4.11: *I-V Curve of MOSFET with L=16 µm, W=80 µm in Saturation Regime*

4.4.2 Extraction of Threshold Voltage and Average Channel Mobility

The $I_{ds,sat}$, $\sqrt{I_{ds,sat}}$ and V_{gs} table is given below:

Table 4.8: *$I_{ds,sat}$, $\sqrt{I_{ds,sat}}$ and V_{gs} Relationship*

V_{gs} (V)	I_{ds} (A) for $W = 40\mu m$	$\sqrt{I_{ds}}$ $(A^{0.5})$ for $W = 40\mu m$	I_{ds} (A) for $W = 80\mu m$	$\sqrt{I_{ds}}$ $(A^{0.5})$ for $W = 80\mu m$
0	4.17×10^{-4}	0.0204	5.10×10^{-4}	0.0226
1	7.14×10^{-4}	0.0267	9.96×10^{-4}	0.0316
2	1.10×10^{-3}	0.0332	1.63×10^{-3}	0.0404
3	1.55×10^{-3}	0.0394	2.38×10^{-3}	0.0488
4	2.06×10^{-3}	0.0454	3.22×10^{-3}	0.0567
5	2.62×10^{-3}	0.0512	4.13×10^{-3}	0.0643
6	3.22×10^{-3}	0.0568	5.11×10^{-3}	0.0715
7	3.86×10^{-3}	0.0621	6.15×10^{-3}	0.0784
8	4.52×10^{-3}	0.0673	7.22×10^{-3}	0.0850
9	5.22×10^{-3}	0.0723	8.33×10^{-3}	0.0912
10	5.94×10^{-3}	0.0770	9.46×10^{-3}	0.0973
11	6.69×10^{-3}	0.0818	1.06×10^{-2}	0.1031
12	7.45×10^{-3}	0.0863	1.19×10^{-2}	0.1089

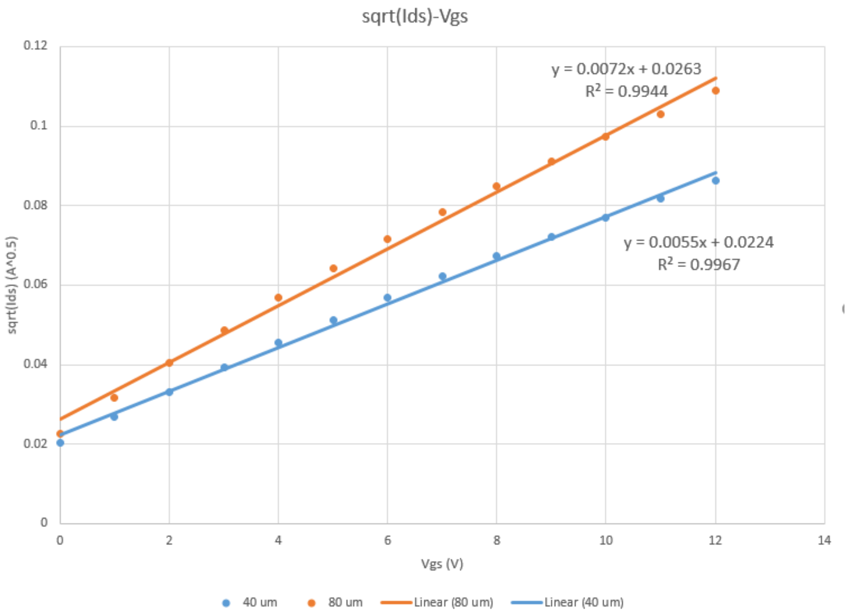

Figure 4.12: *$\sqrt{I_{ds,sat}}$ and V_{gs} Relationship*

Figure 4.12 shows the $\sqrt{I_{ds,sat}}$ and V_{gs} relationship curve and two linear fitting functions.

For MOSFET #1, the linear equation is $y = 0.0055x + 0.0224$. The threshold voltage $V_{th,1}$ is the intercept of X-axis, which is -4.07 (V). Then the thickness of the oxide is the average in MOS capacitor part, which is 577.7 (A). And the oxide capacitance is

$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}} = 5.97 \times 10^{-8}\ (F/cm^2) \tag{4.16}$$

Then the mobility is:

$$\begin{aligned} Slope_1 &= \sqrt{\frac{\mu_1 C_{ox} W}{2L}} = 0.055 \\ \mu_1 &= \frac{2 * 16 * 0.0069^2}{5.97 \times 10^{-8} \times 40} = 637.99\ (cm^2/V \cdot s) \end{aligned} \tag{4.17}$$

For MOSFET #2, the linear equation is $y = 0.0072x + 0.0263$. The threshold voltage $V_{th,2}$ is the intercept of X-axis, which is -3.65 (V). Then the mobility is:

$$\begin{aligned} Slope_2 &= \sqrt{\frac{\mu_2 C_{ox} W}{2L}} = 0.0072 \\ \mu_2 &= \frac{2 * 16 * 0.0072^2}{5.97 \times 10^{-8} \times 40} = 694.67\ (cm^2/V \cdot s) \end{aligned} \tag{4.18}$$

4.4.3 Saturation Velocity(V_S)

The saturation velocity calculation is based on the equation:

$$I_{ds,sat} = v_{sat} C_{ox} W (V_{gs} - V_{th}) \tag{4.19}$$

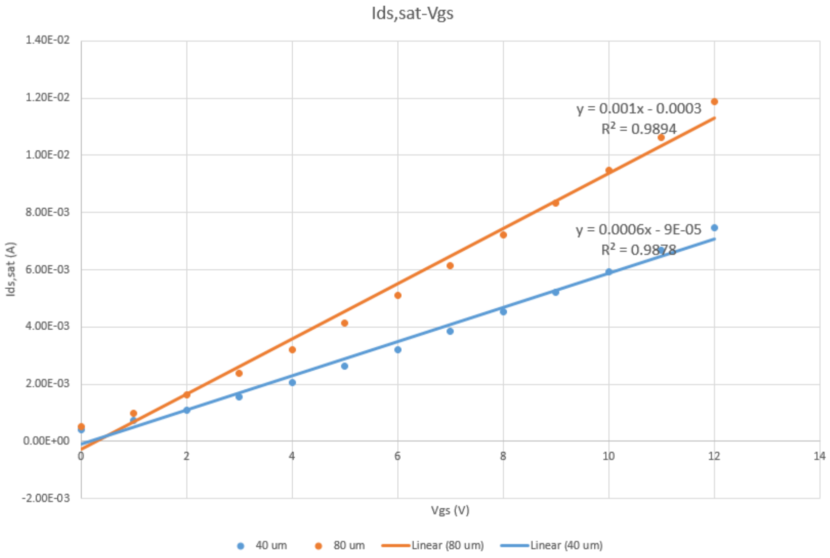

Figure 4.13: *$I_{ds,sat}$ and V_{gs} Relationship*

Figure 4.13 shows the $I_{ds,sat}$ and V_{gs} relationship.
For $W = 40\ \mu m$ case,

$$\begin{aligned} y_1 &= 0.0006x_1 - 9 \times 10^{-5} \\ Slope_1 &= v_{sat,1} C_{ox} W \\ v_{sat,1} &= \frac{Slope_1}{C_{ox} W} = \frac{0.0006}{5.97 \times 10^{-8} \times 4 \times 10^{-3}} = 2.51^6\ (cm/s) \end{aligned} \tag{4.20}$$

For $W = 80\ \mu m$ case,

$$\begin{aligned} y_2 &= 0.001x_1 - 0.0003 \\ Slope_2 &= v_{sat,2}C_{ox}W \\ v_{sat,2} = \frac{Slope_2}{C_{ox}W} &= \frac{0.001}{5.97 \times 10^{-8} \times 8 \times 10^{-3}} = 2.10^6\ (cm/s) \end{aligned} \tag{4.21}$$

4.4.4 Transconductance(g_m) of MOSFET

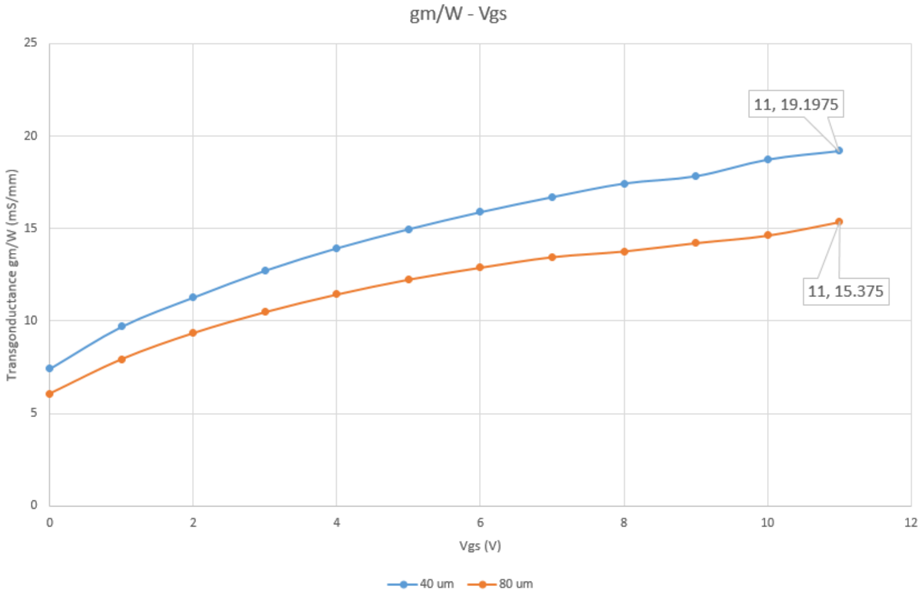

Figure 4.14: *Transconductance g_m and V_{gs} Relationship*

The table below gives the value of g_m and corresponding V_{gs} for both two MOSFETs.

Figure 4.14 shows the transconductance g_m and V_{gs} relationship. From the figure, we can find that the maximum g_m for the two MOSFETs are:

$$\begin{aligned} g_{m,max,40\mu m} &= 0.77\ mS \qquad at\ V_{gs} = 11\ (V) \\ g_{m,max,80\mu m} &= 1.23\ mS \qquad at\ V_{gs} = 11\ (V) \end{aligned} \tag{4.22}$$

Table 4.9: *Transconductance* g_m *&* V_{gs}

V_{gs} (V)	$I_{ds,sat,40\mu m}$ (mA)	$g_{m,40\mu m}$ (mS)	$I_{ds,sat,80\mu m}$ (mA)	$g_{m,80\mu m}$ (mS)
0	0.417	0.298	0.510	0.485
1	0.714	0.388	0.996	0.635
2	1.100	0.452	1.630	0.748
3	1.550	0.510	2.380	0.839
4	2.060	0.558	3.220	0.915
5	2.620	0.599	4.130	0.980
6	3.220	0.636	5.110	1.030
7	3.860	0.668	6.150	1.080
8	4.520	0.698	7.220	1.100
9	5.220	0.714	8.330	1.400
10	5.940	0.749	9.460	1.700
11	6.690	0.768	10.600	1.230

4.4.5 Output Conductance(g_d)

In this section, I use the two I_{ds} value at $V_{ds} = 14\ V\ and\ 4V$ to calculate the g_d value. Table below shows the g_d and V_{gs} relationship.

Table 4.10: *Output Conductance* g_d *&* V_{gs}

V_{gs} (V)	$g_{d,40\mu m}$ (mS)	$g_{d,80\mu m}$ (mS)
0	0.0118	0.0102
1	0.0151	0.0150
2	0.0195	0.0210
3	0.0245	0.0289
4	0.0340	0.0424
5	0.0522	0.0693
6	0.0783	0.1092
7	0.1110	0.1591
8	0.1490	0.2171
9	0.1910	0.2804
10	0.2370	0.3496
11	0.3010	0.4236

Figure 4.15 shows the output conductance g_d and V_{gs} relationship. The maximum value of g_d is as:

$$\begin{aligned} g_{d,max,40\mu m} &= 0.3010\ mS \qquad at\ V_{gs} = 11\ (V) \\ g_{d,max,80\mu m} &= 0.4236\ mS \qquad at\ V_{gs} = 11\ (V) \end{aligned} \tag{4.23}$$

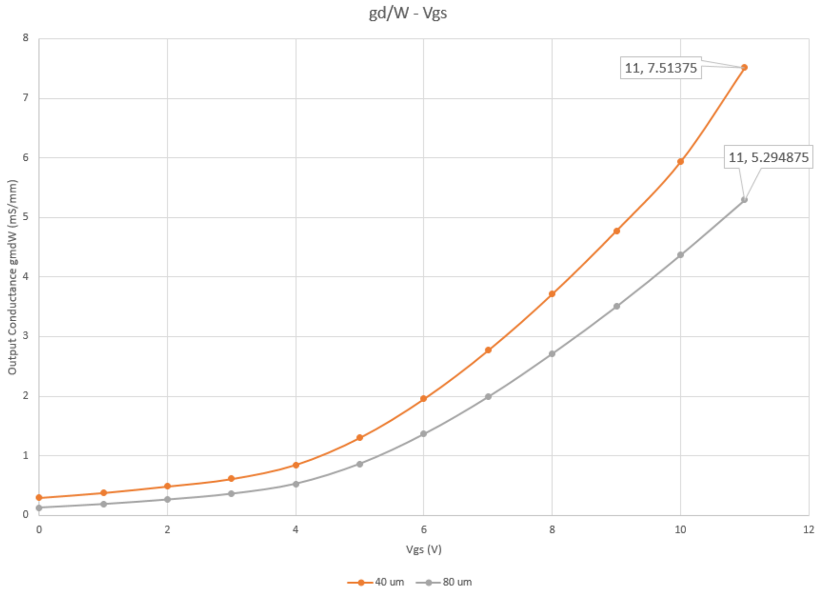

Figure 4.15: *Output Conductance g_d and V_{gs} Relationship*

4.4.6 $\frac{g_m}{g_d}$ and Voltage Swing

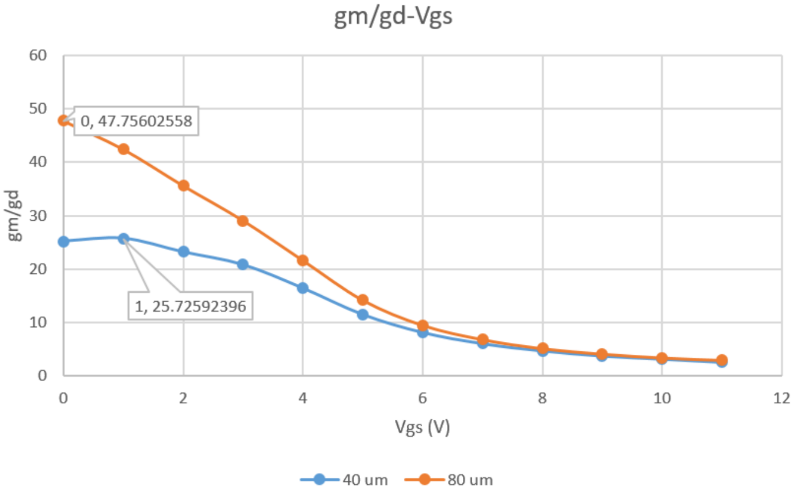

Figure 4.16: $\frac{g_m}{g_d}$ *and V_{gs} Relationship*

Figure 4.16 shows the $\frac{g_m}{g_d}$ and V_{gs} relationship. For 40 μm device, the maximum value of $\frac{g_m}{g_d}$ value is 27.73, and its 90% value is 24.95, however, since the curve doesn't shows the other side, the estimated voltage swing is 2 (V). For 80 μm device, the maximum value of $\frac{g_m}{g_d}$ value is 47.76, and its 90% value is 42.98, the estimated voltage swing is also 2 (V).

4.4.7 Channel Conductance(g_c) and Extraction of Mobility in Linear Regime

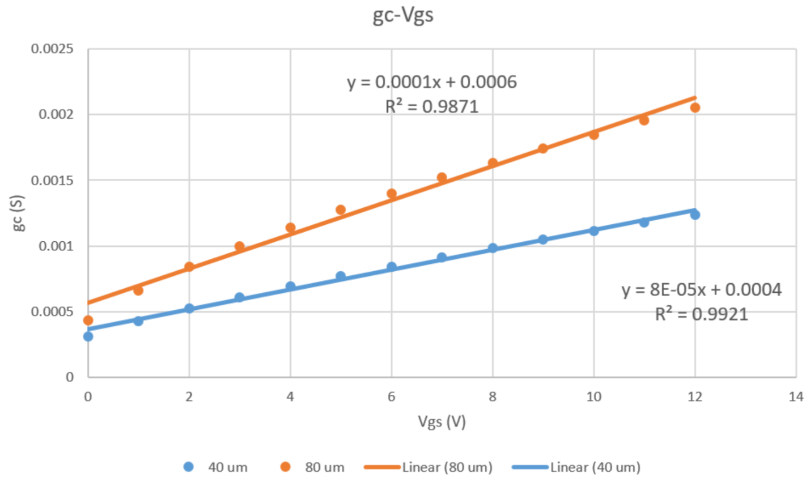

Figure 4.17: *g_c and V_{gs} Relationship*

Figure 4.17 shows the conductance g_c to V_{gs} relationship in linear region for two MOSFETs. Here I used $V_{ds,2} = 0.1\ V$ and $V_{ds,1} = 0\ V$ to calculate g_c. The mobility can be obtained by applying equations:

$$\begin{aligned} g_c &= \frac{\mu_{lin} C_o W}{L}(V_{gs} - V_{th}) \\ \mu_{lin} &= \frac{L \times Slope}{C_o W} \end{aligned} \tag{4.24}$$

Then for 40 μm MOSFET, the mobility is $\mu_{lin,1} = 536\ (cm^2/V \cdot s)$ and $V_{th,1} = -5\ (V)$. For 80 μm MOSFET, the mobility is $\mu_{lin,2} = 335\ (cm^2/V \cdot s)$ and $V_{th,2} = -6\ (V)$.

5. Discussion

5.1 Resistor

For sheet resistance measurements, R_{sh} of R_{400}, R_{800}, R_{5400} are almost the same, which is around 5.5 ($\Omega/\square$), which means that it has a good consistency and the doping level are uniform in this region. However, for the TLM-20 case, the value of R_{sh} is much smaller than the previous one, perhaps its because the insufficient doping concentration in this area and the bend part effect, or may be it is because the method we use eliminated some of the effect of resistance in the measurement circuit.

5.2 PN Diode

For PN diode part, the $I-V$ curve shows a good electric characteristic of the device as it in theory. The electric parameters extracted from the two diodes are quite similar, which shows the uniformity of the wafer in diode part. The built-in potential V_{bi} of both two diodes are about 0.214 V, which is a reasonable value. And for ideality factor n, n_3 is much more larger than n_1 and n_2 in both cases, which is because of the imperfect process during fabrication. The reverse saturation current I_0 is in nA level, which is a decent value.

5.3 MOS Capacitor

For MOS capacitors, the graph of $C-V$ is not good because that the tail part goes up when the bias voltage get higher. For extracted parameters, the thickness, doping concentration and oxide charge value are similar for the two capacitors. For the thickness of oxide, it's about 600 (A), for N_{sub}, it's in 10^{15} level, and for N_f, it's in 10^{11} level, are these values are in reasonable range.

5.4 MOSFET

For MOSFET part, the $I-V$ curves look perfect as in theory. However, when calculating the value of transconductance g_m, output conductance g_d, its value are kind of weird and its trend is different with graph in theory. It seems that the peak value of V_{gs} for these two parameters are larger than the measured range. Therefore, for the voltage swing part, there is no way to calculate it, then the estimation and some imagination are used for that section. For the other calculated parameters, the value of them are reasonable.

6. Conclusion

In EE504L, we can not only gain knowledge from the slides in the class but also in the lab session and get a deep experience in industry fabrication process.

In class we learned theoretical knowledge about IC fabrication, IC testing, CMOS fabrication process and advanced CMOS technology while in lab session, we can get hand-on experience and building our own wafer. In the lab we can learn the fabrication process step by step, which could help us to get a better command of the knowledge learned in class.

Prof. Kian Kaviani has valuable experience in industry which give us a clear view of semiconductor industry and also help us to learn knowledge better. TA Jihan Chen is a definitely a fantastic TA with patience and technique, he helped us a lot in the lab session.

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