EE577A Lab2 Report

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Schematic Design

Single SRAM bit

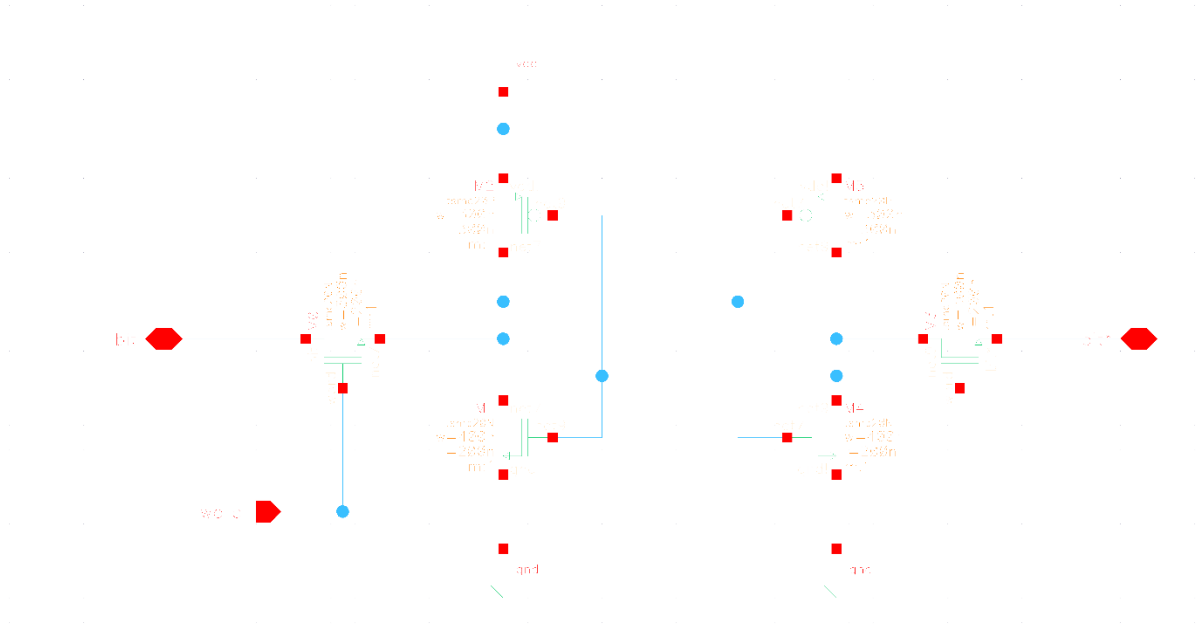


Figure 1: Schematics of Single SRAM Bit

Figure 1 shows the schematics of a single SRAM bit, the size of NMOS in the latch is 4/2, and the size of PMOS in the latch is 3/3, the size of the access NMOS is 3/2. The reason I set them this way is shown in next section

Single Cell Sizing Optimization

To minimize the area of a single cell and improve its timing delay, I tried different combinations of sizing and the combination above has the best tradeoff for area and delay. The testing circuit will show below. The first one is the reading test circuit and the second one is the writing test circuit.

Table 1 shows the read and write delay for each sizing combination, all tests have included the dummy capacitors.

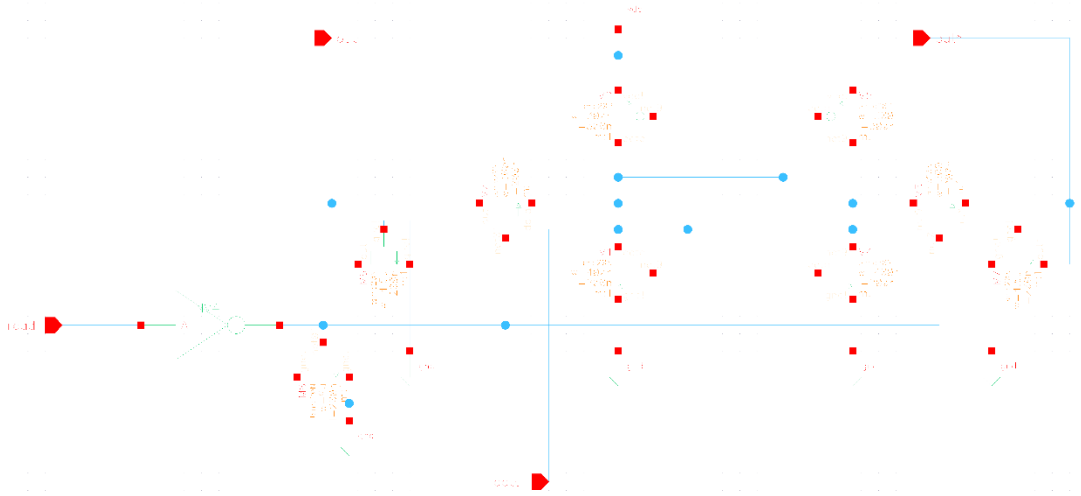


Figure 2: Reading Bit Test Circuit

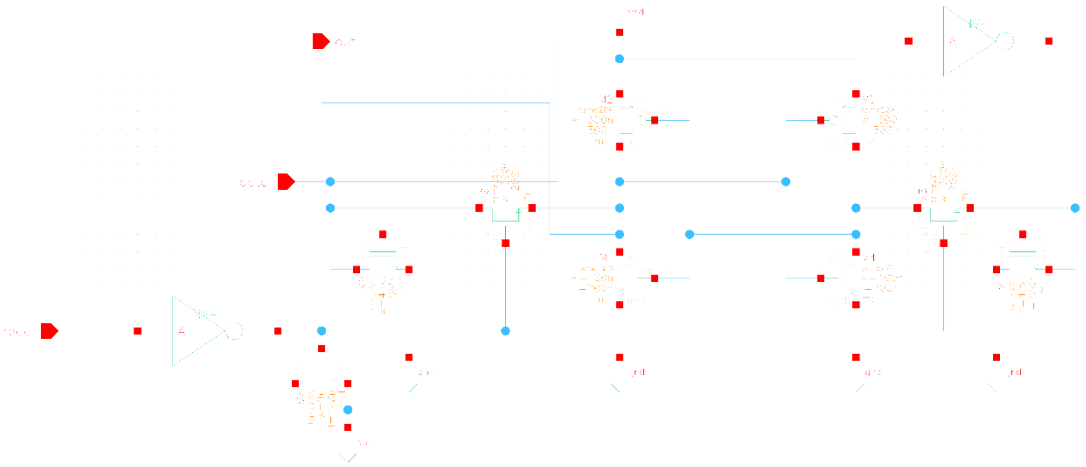


Figure 3: Writing Bit Test Circuit

Size of NMOS	Size of PMOS	Size of Access NMOS	Read 0 (ps)	Read 1 (ps)	Write 0 (ps)	Write 1 (ps)
6λ/2λ	4λ/3λ	4λ/2λ	82.4	96.6	24.2	99.9
6λ/2λ	5λ/3λ	4λ/2λ	82.3	96.6	27.3	104.0
6λ/2λ	3λ/3λ	4λ/2λ	82.3	96.4	21.4	96.2
5λ/2λ	3λ/3λ	4λ/2λ	82.3	96.4	19.6	90.6
5λ/2λ	3λ/3λ	3λ/2λ	71.9	82.9	23.5	94.1
4λ/2λ	3λ/3λ	3λ/2λ	71.8	82.9	21.4	87.4

Table 1: Read & Write Delay of Different Sizing Combinations

Precharge Circuit

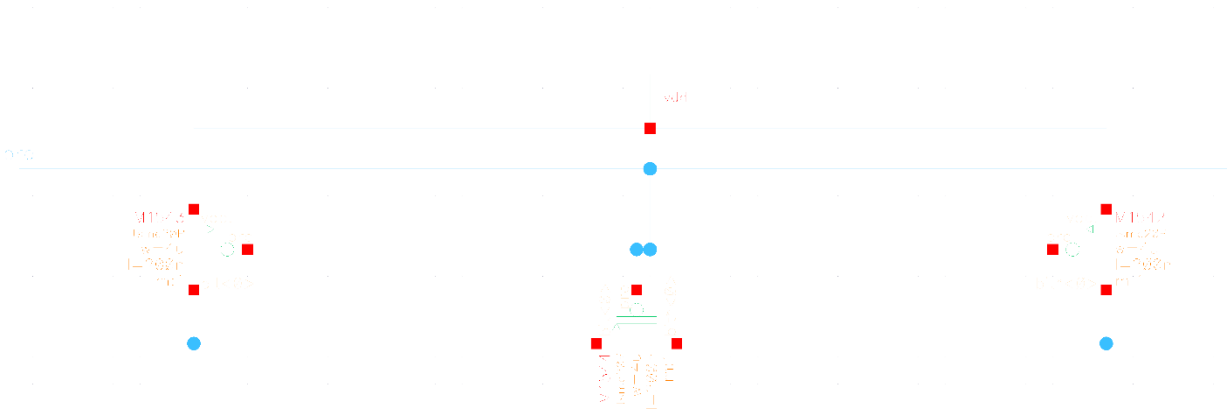


Figure 4: Precharge Circuit

Figure 4 shows the schematics of the precharge circuit. All the PMOS transistors are sized as 40 λ/2 λ to assure it has a strong ability to pull up the whole bitline to Vdd.

Single Bank Schematics

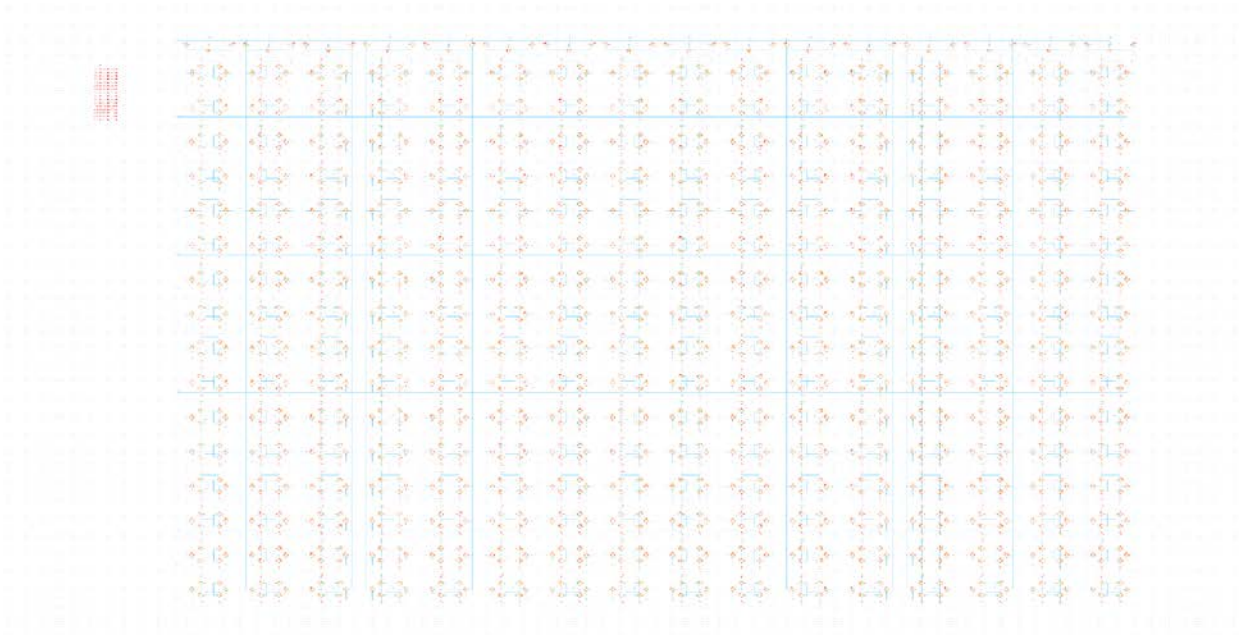


Figure 5: Single Bank Schematics

Figure 5 shows the schematics of the single bank. It contains the 16X16 bit SRAMs and 16 precharge circuits for each bitline.

2-to-4 Decoder (Bank MUX)

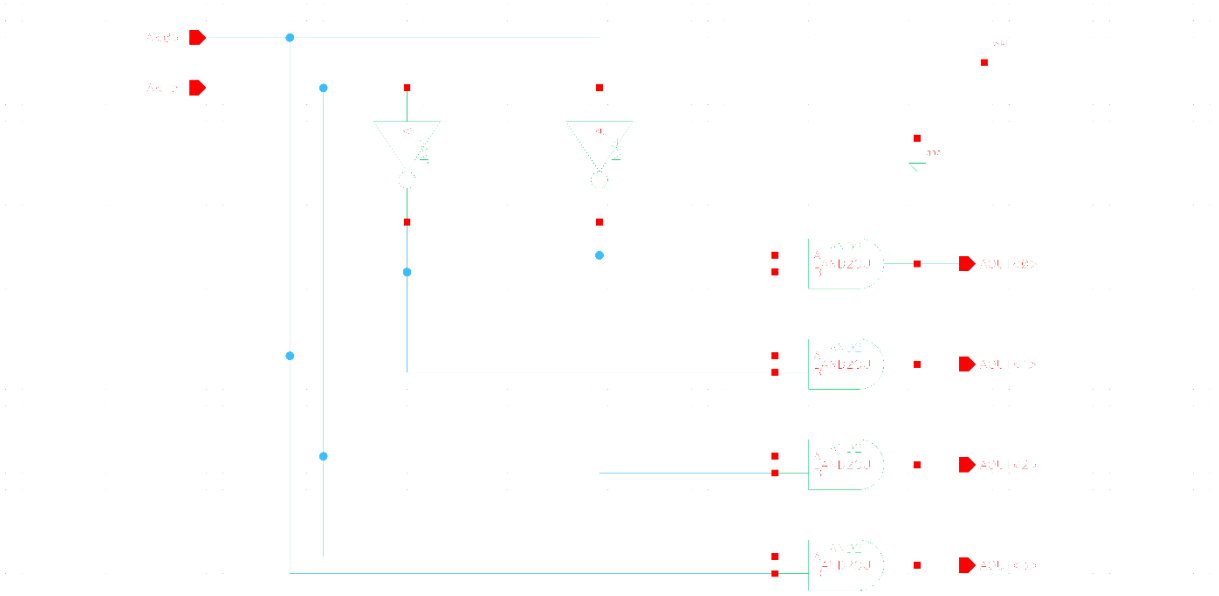


Figure 6: 2-to-4 Decoder

Figure 6 shows the schematics of 2-to-4 decoder, it is also work as the multiplexer to choose one of the four banks.

4-to-16 Decoder (Word Line MUX)

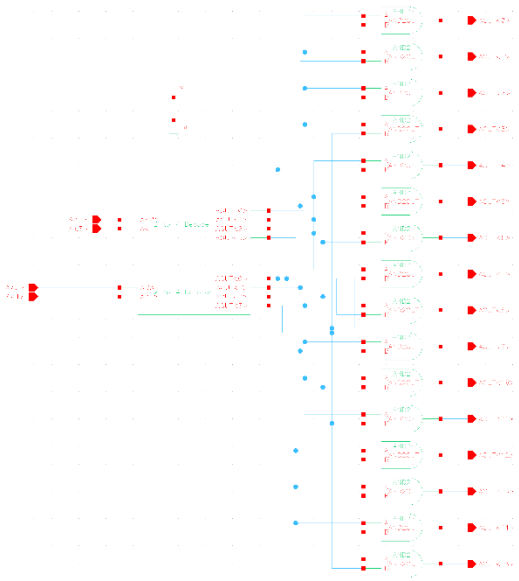


Figure 7: 4-to-16 Decoder

Figure 7 shows the schematics of the 4-to-16 decoder, which is used for choosing which wordline to use in doing read and write operations.

MUX Transistor Circuit

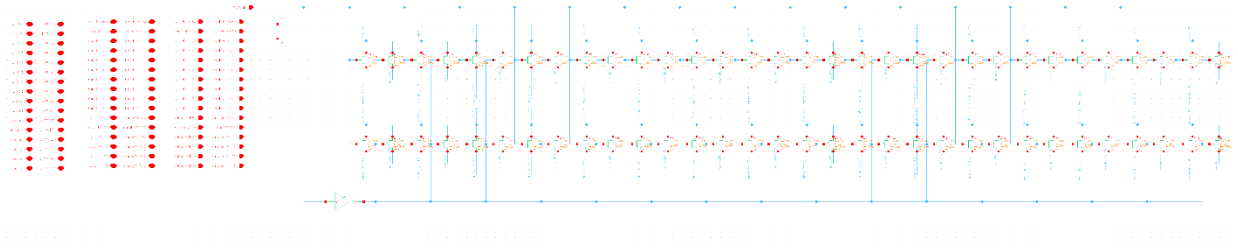


Figure 8: MUX Transistor Circuit

Figure 8 shows the schematics of the MUX transistor circuit. For read path, it uses the PMOS to transmit the signal, and its size is 20 λ/2 λ. And for write path, it uses the NMOS, and its size is 30 λ/2 λ.

Sense Amplifier

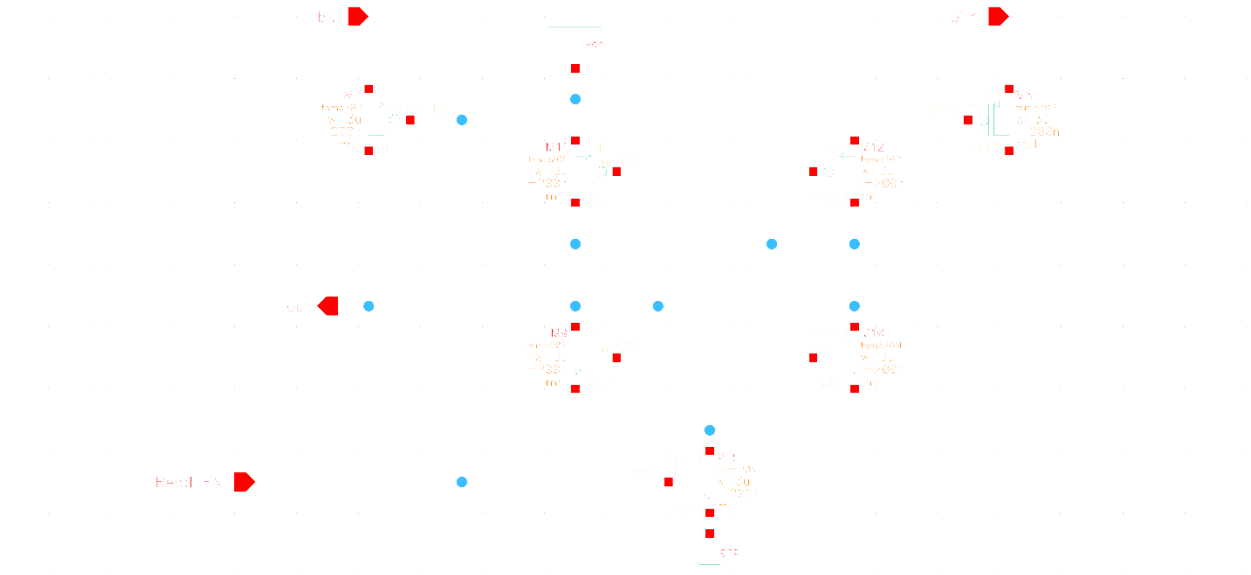


Figure 9: Sense Amplifier Circuit

Figure 9 shows the schematics of the sense amplifier circuit. The size for all the transistors are 30 λ/2 λ to make sure that the strength of the transistors is strong enough to pull up and pull down.

Write Path

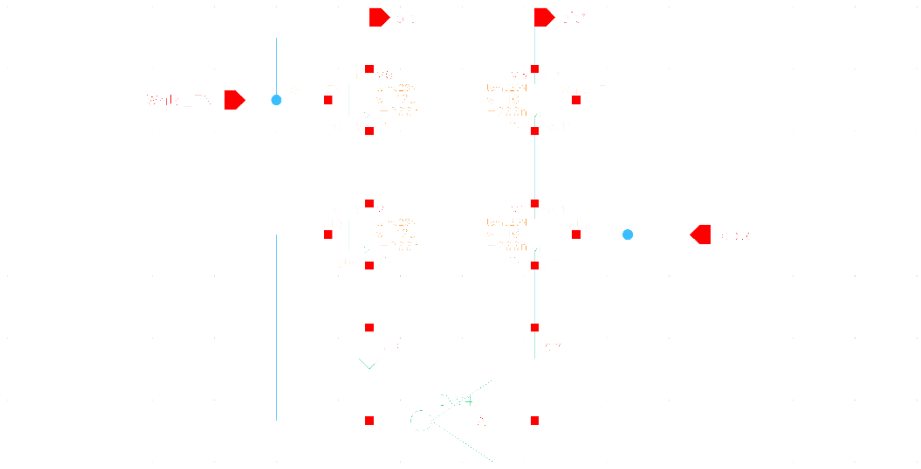


Figure 10: Write Path Circuit

Figure 10 shows the schematics of the write path circuit. For all the NMOS transistors, their size is 20 λ/2 λ.

Single SRAM Bit Test with Sense Amplifier and Write Path

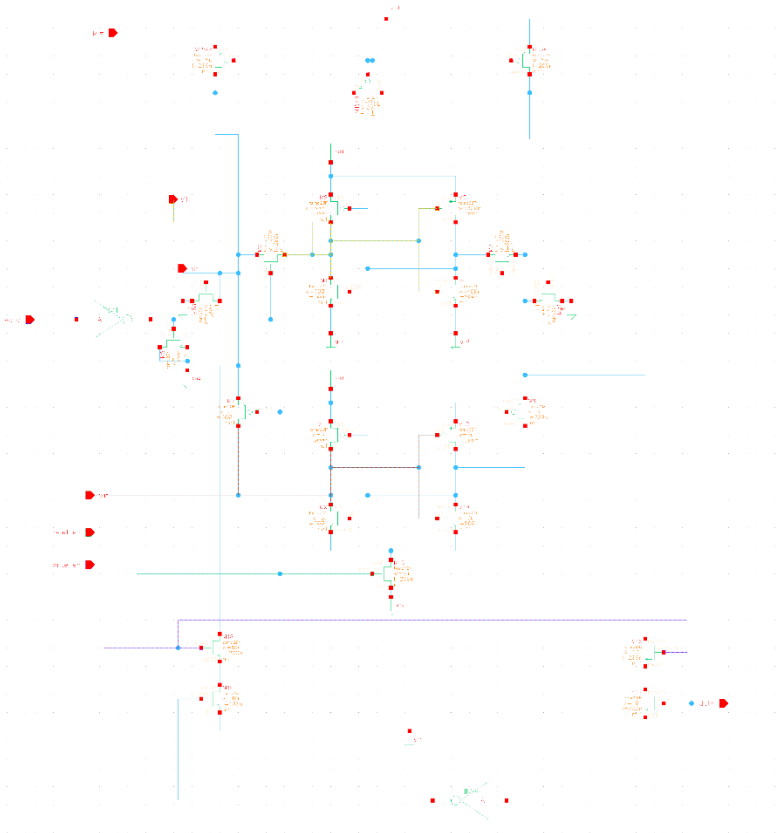


Figure 11: Single SRAM Bit Test with Sense Amplifier and Write Path

Figure 11 shows the schematics of a single SRAM bit test circuit with the sense amplifier and the write path.

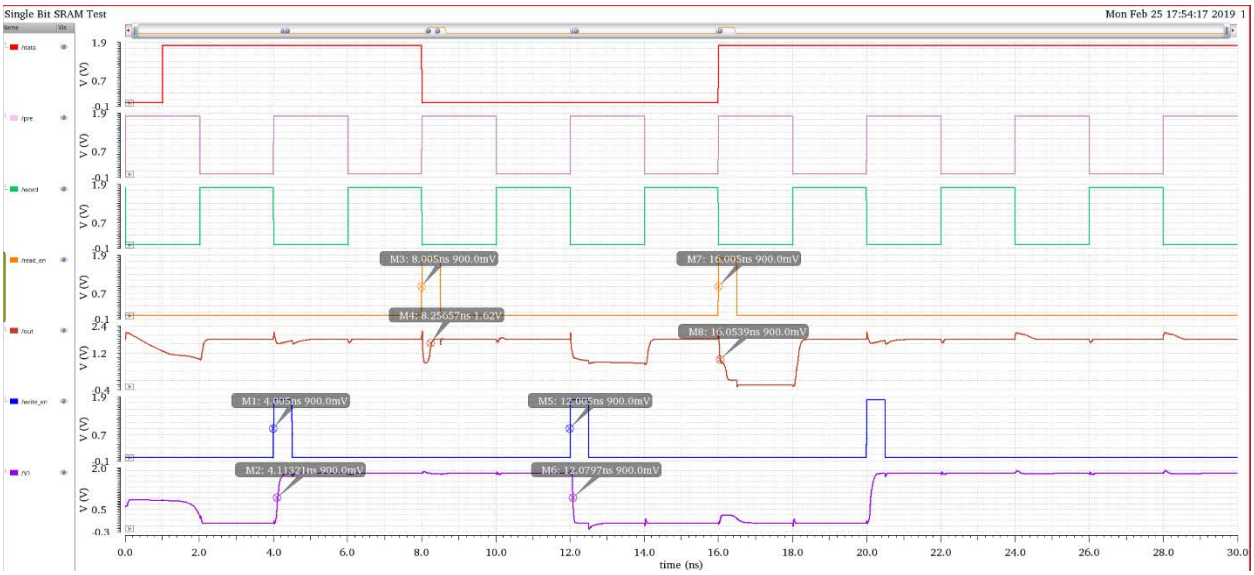


Figure 12: Output of A Single Bit SRAM

Figure 12 shows the test result of a single bit SRAM. The operation did by this SRAM is write 1 -> read 1 -> write 0 -> read 0 -> write 1. For the write time, it's 108.2 ps for writing 1, and it's 74.7 ps for writing 0. For read time, it's 251.6 ps for read 1, and it's 251.7 ps for reading 1, and it's 48.9 ps for reading 0.

DFF

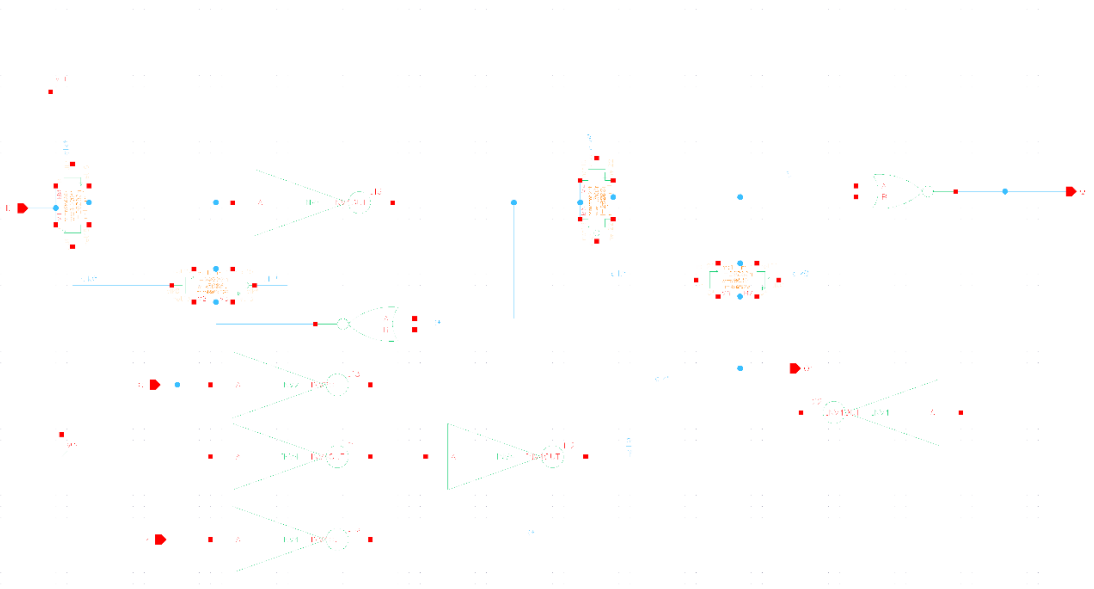


Figure 13: D-Flip-Flop Circuit

Figure 13 shows the schematics of the D-Flip-Flop.

Complete 1024-Bit SRAM Circuit

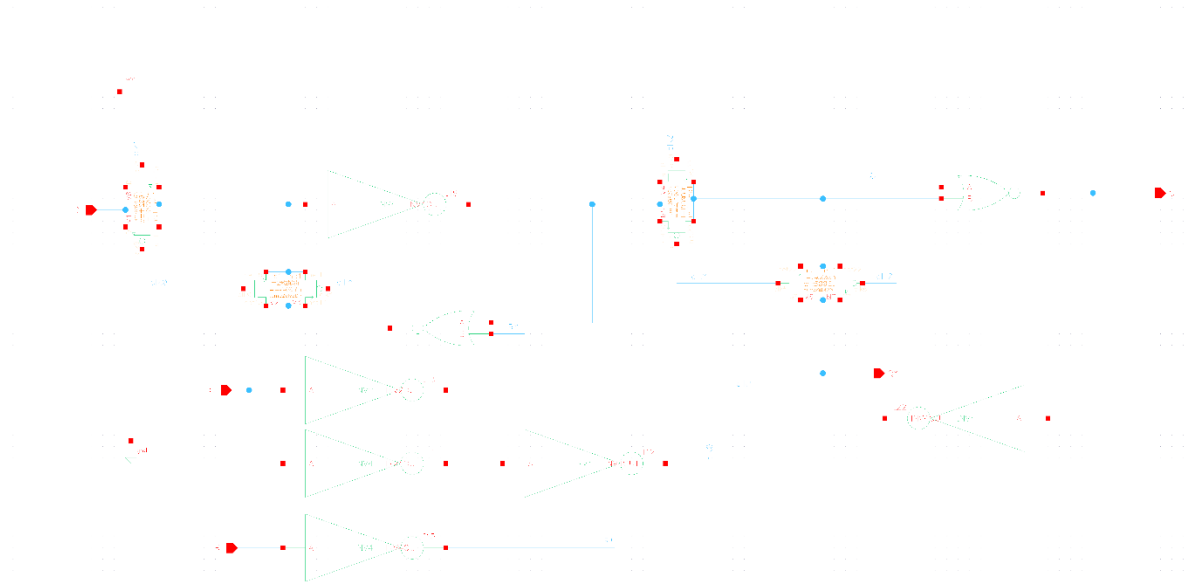


Figure 14: SRAM Schematic

Figure 14 shows the schematics of the SRAM.

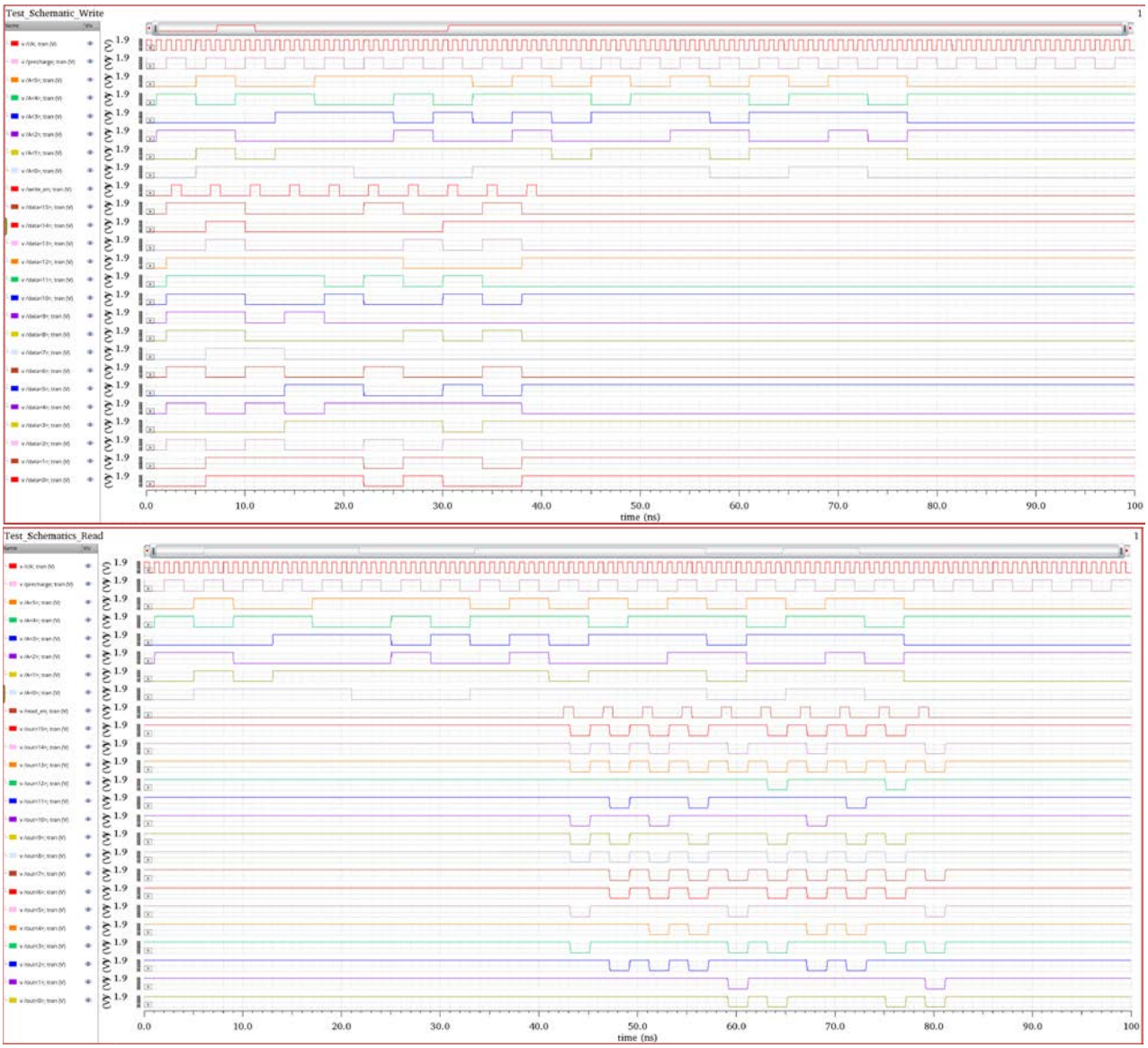


Figure 15: Schematic Test

Figure 15 shows the test result of the schematic SRAM. Firstly, I write the input digits with the sequence of 6->7->8->9->0->1->2->3->4->5 to 10 different address. And then I read them with the order of my USC ID as 8->0->9->5->6->3->9->5->3->6. It is properly functioning.

Layout Part

SRAM_Bit Layout

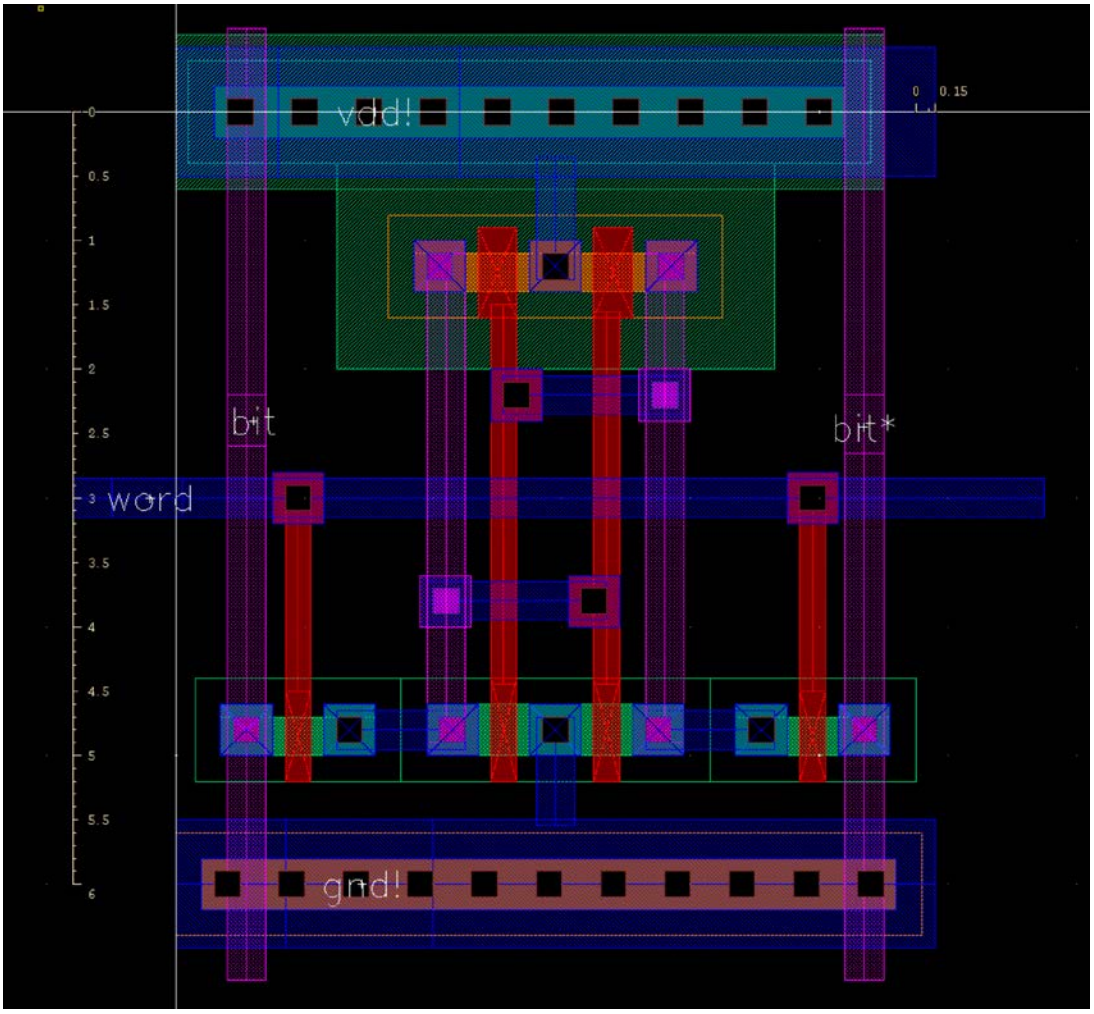


Figure 16: Layout of SRAM_Bit

Figure 16 shows the layout of a single bit SRAM.

Bank Layout

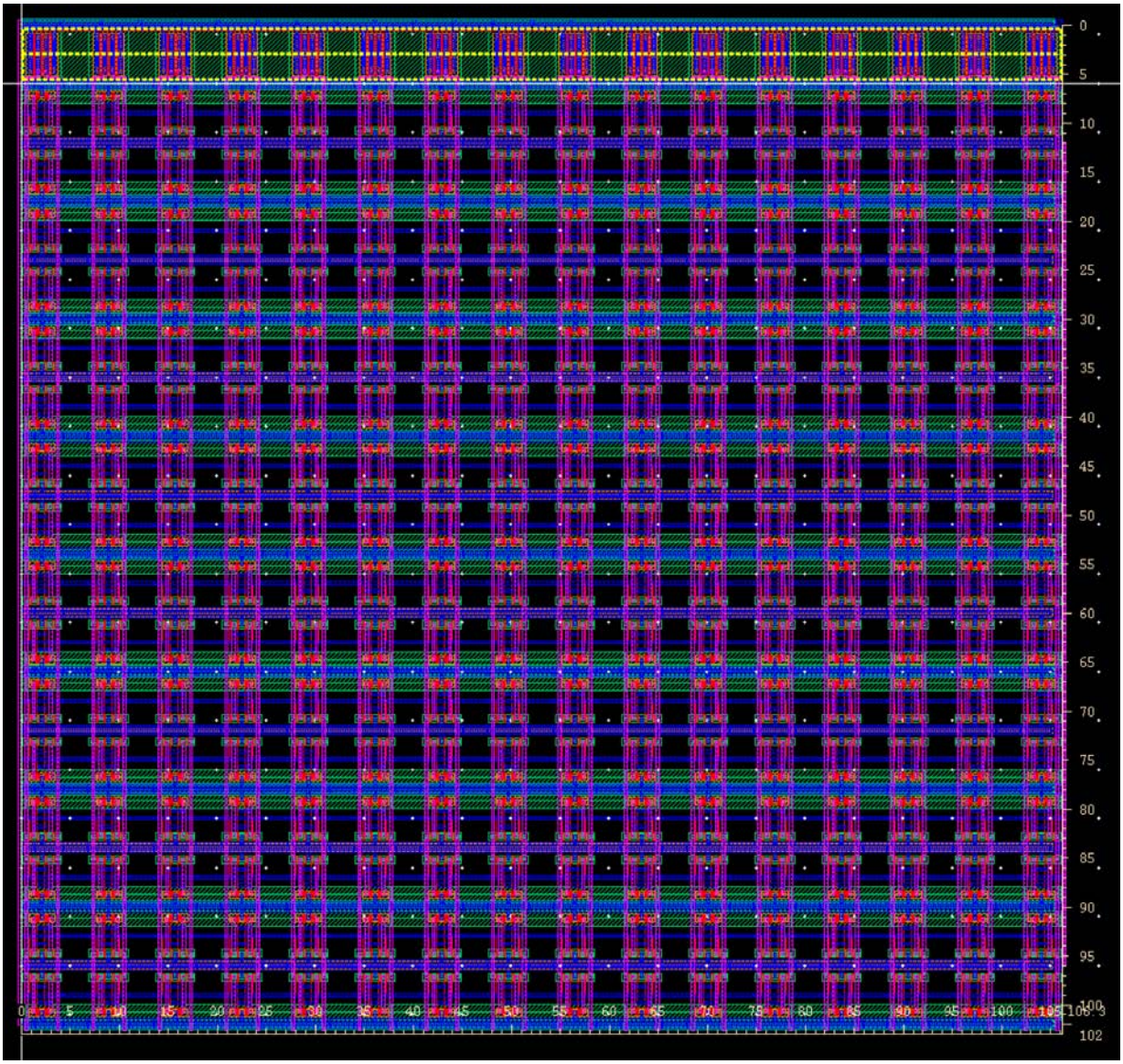


Figure 17: Layout of Bank

Figure 17 shows the layout of a 256-bit bank.

MUX Layout

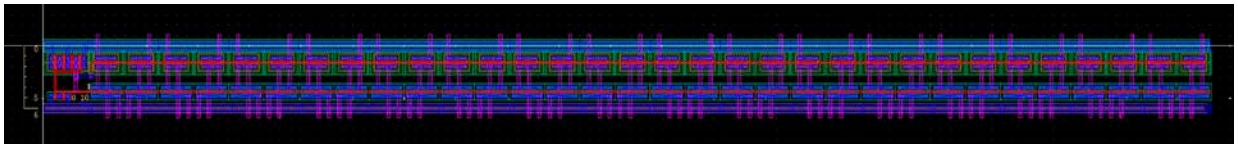


Figure 18: Layout of MUX Transistors

Figure 18 shows the layout of the MUX transistors.

Sense Amplifier Layout

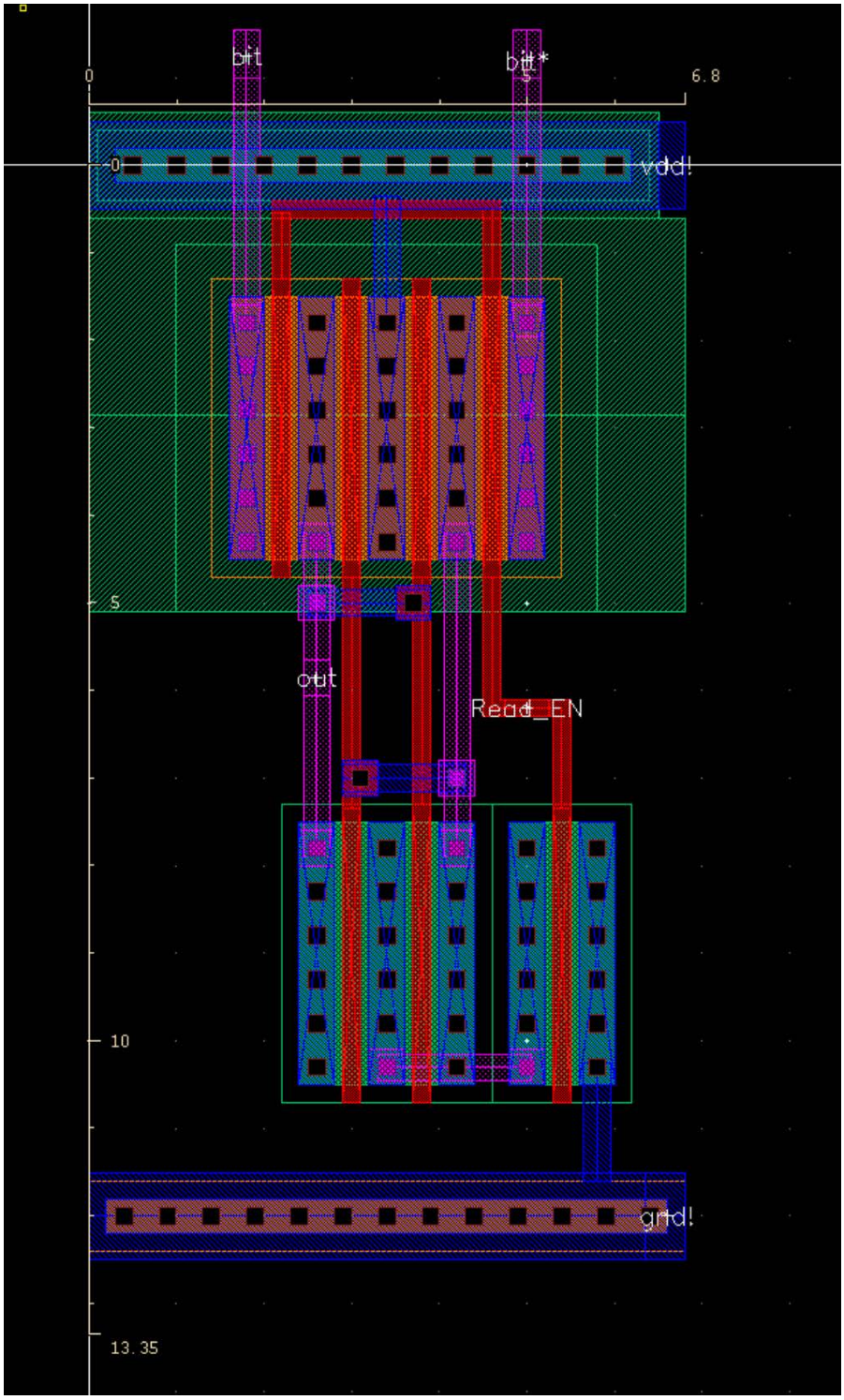


Figure 19: Layout of Sense Amplifier

Figure 19 shows the layout of the sense amplifier.

Write Path Layout

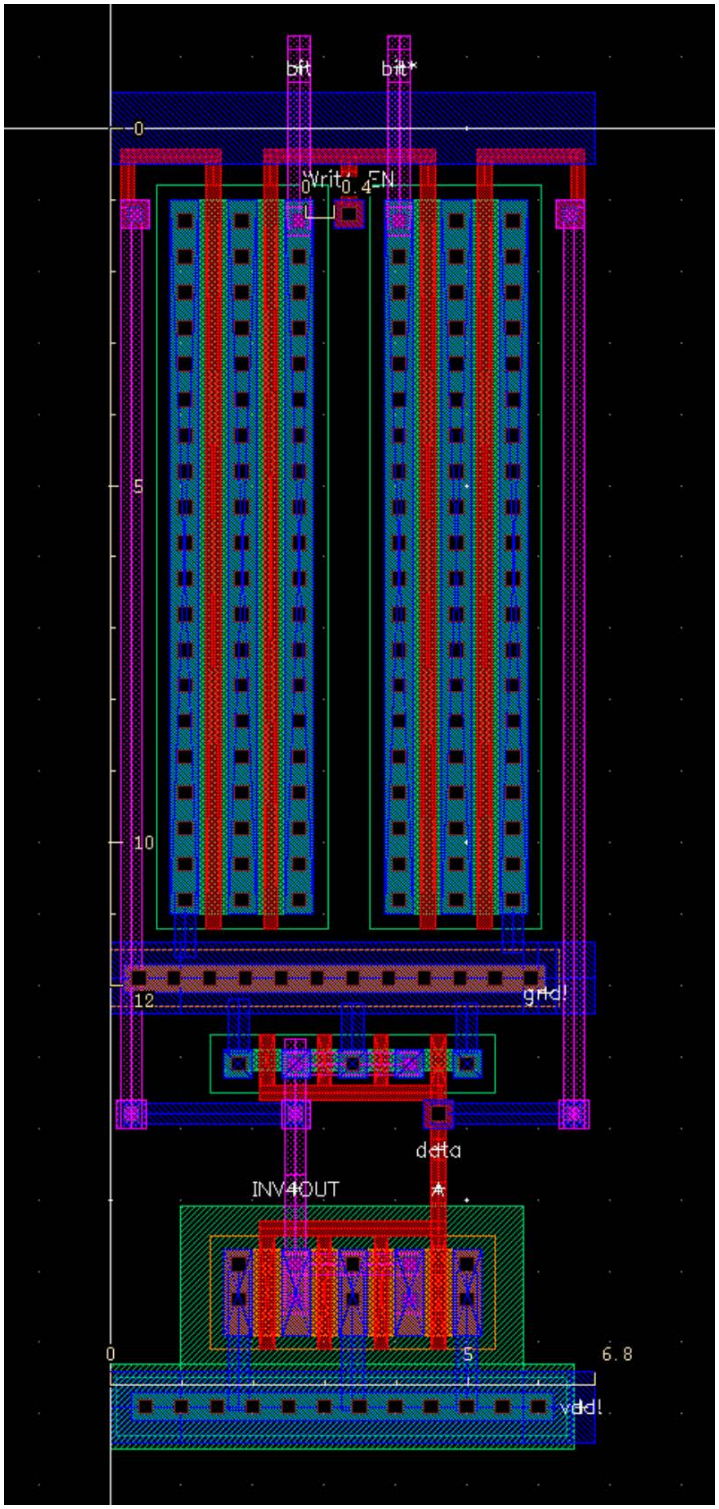


Figure 20: Layout of Write Path

Figure 20 shows the layout of the write path.

2-to-4 Decoder Layout

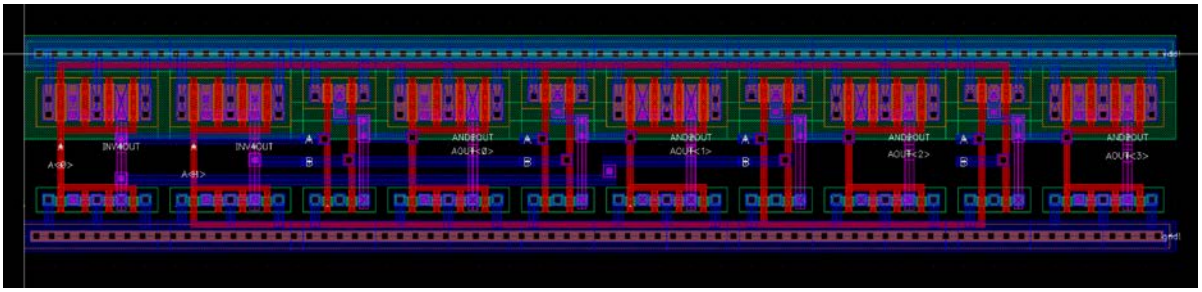


Figure 21: Layout of 2-to-4 Decoder

Figure 21 shows the layout of the 2-to-4 decoder.

4-to-16 Decoder Layout

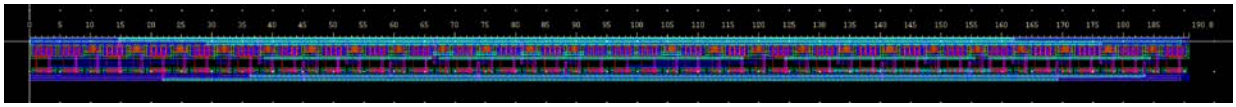


Figure 22: Layout of 4-to-16 Decoder

Figure 22 shows the layout of the 4-to-16 decoder.

DFF Layout

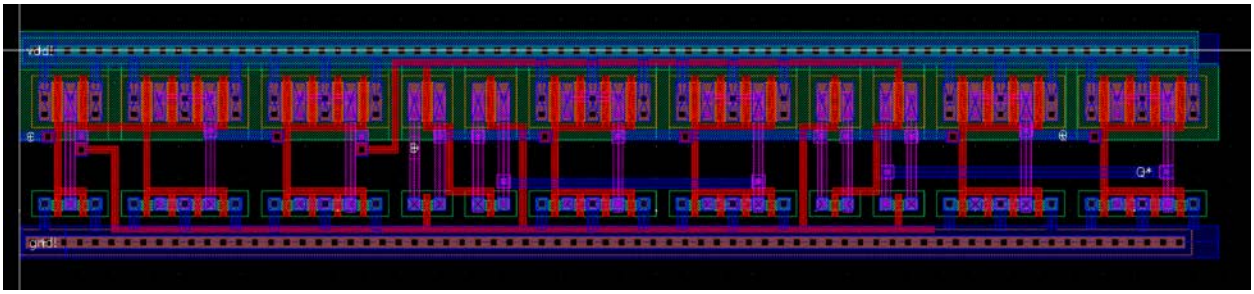


Figure 23: Layout of DFF

Figure 23 shows the layout of the DFF.

1024-Bit SRAM Layout

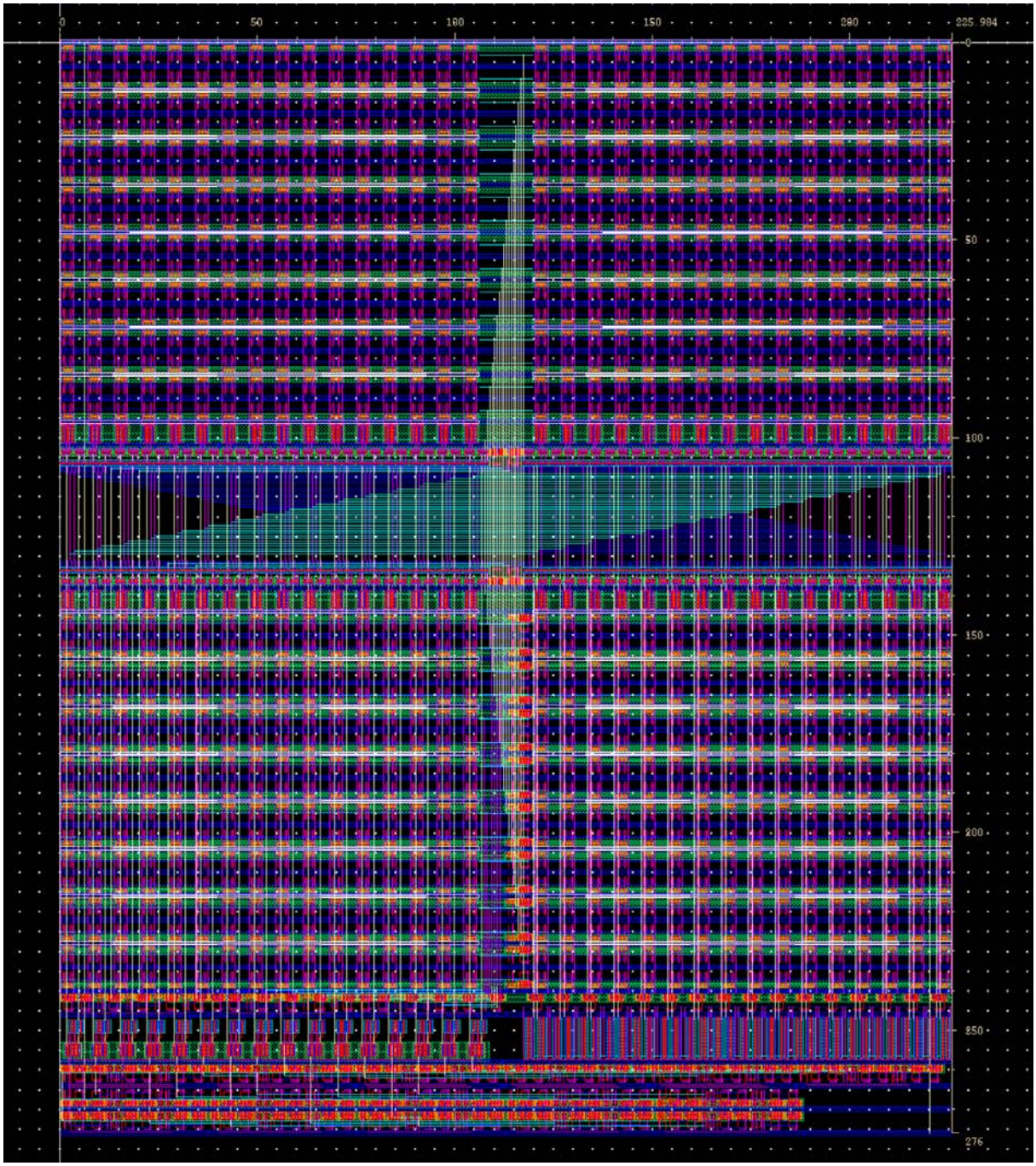


Figure 24: Layout of 1024-Bit SRAM

Figure 24 shows the layout of the SRAM. The area of the SRAM is 276 µm X 226 µm, which is 62376 µm^2.

LVS Test Result

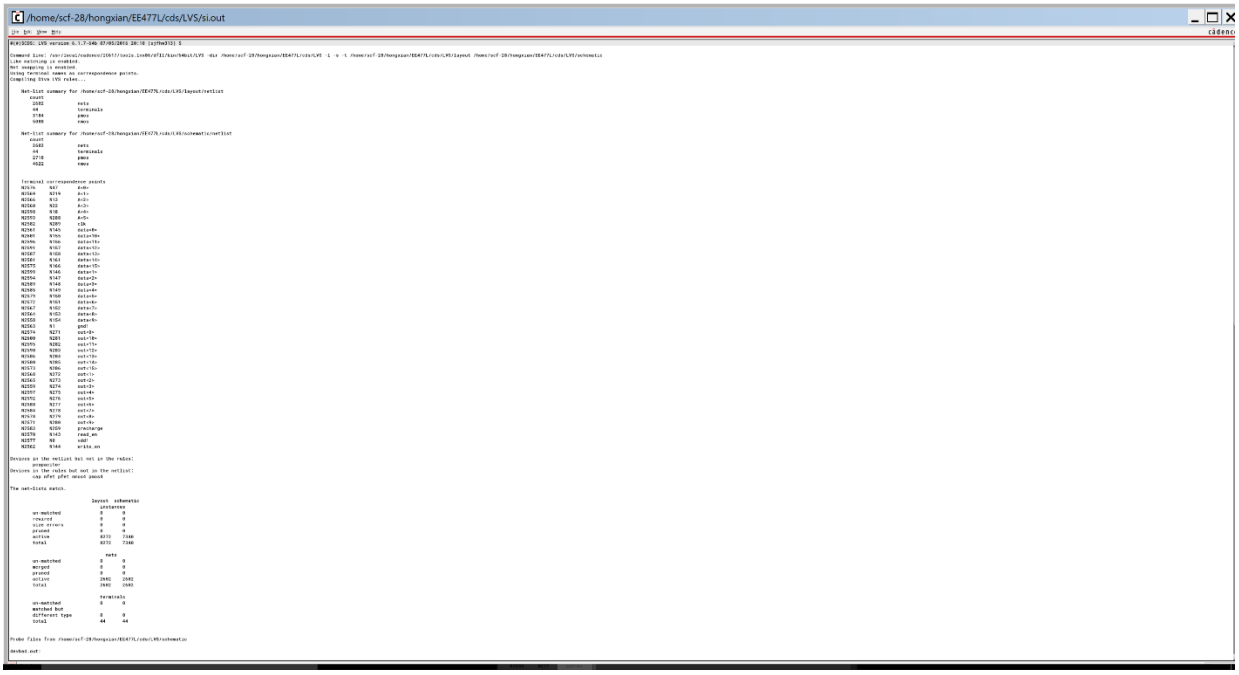
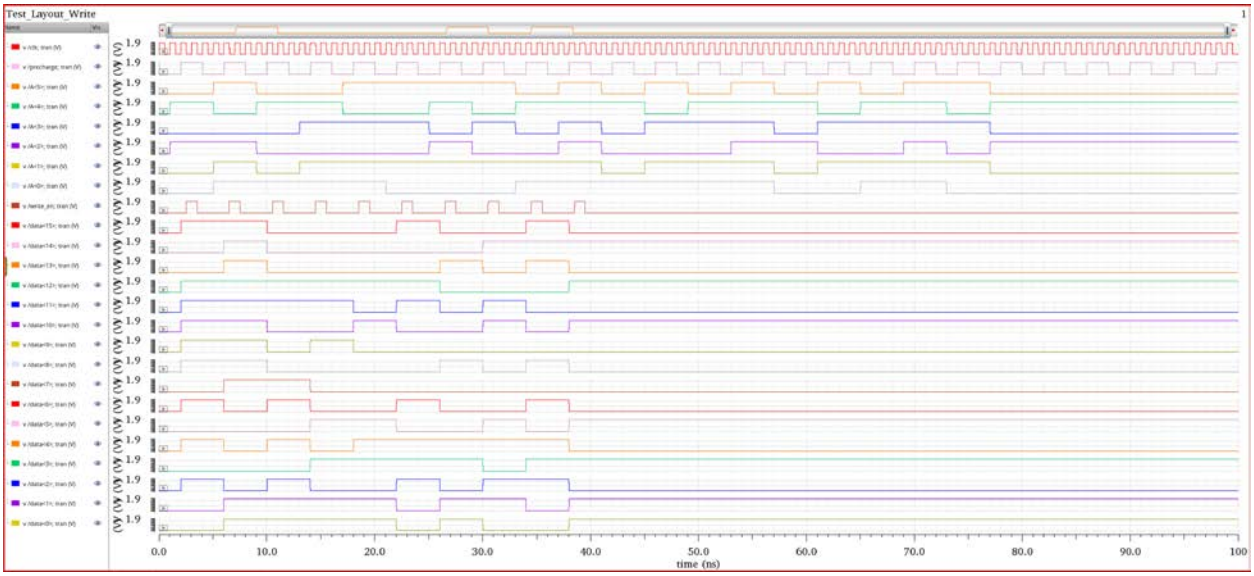


Figure 25: LVS Test

Figure 25 shows the LVS test result.

Layout Test



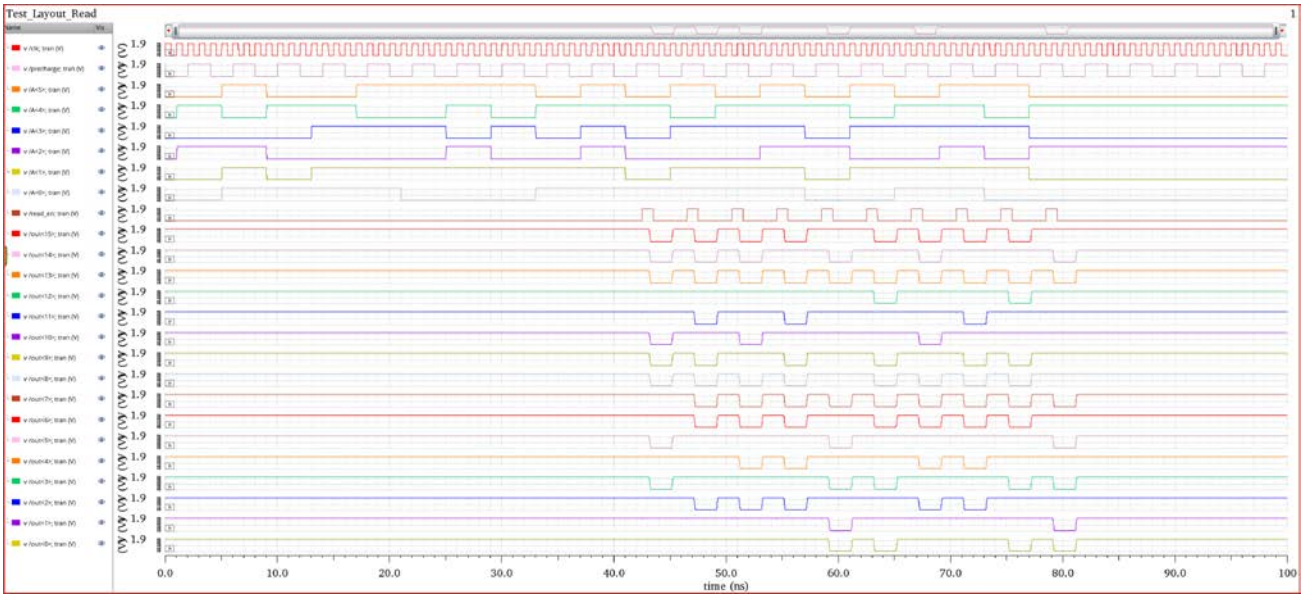


Figure 26: Layout Test

Figure 26 shows the test result of the layout circuit, it is exactly the same with the schematic one.

Key Parameters

The area of the circuit is 62376 µm^2, the read time delay is 1051.7 ps, and the write time delay is 908.2 ps.

Read Me

For the test bench, the address of 1 and 3 are the same, so since I write 3 after 1, my 1 would be overwritten by 3. But since my USC ID doesn't have a number 1, so it doesn't happen any problem in the output.

For high resolution pictures, they are compressed in the other .tar file.