EE582 Final Project

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Contents

1 Introduction

Everyday we receive a huge amount of visual information from outside. One of the early human visual processes is to identify occluding contours and to distinguish an object from its surrounding background. Then border ownership detection is quite important topic in building neuron network[1].

In this project, we have to build an electronic neuron or a small neural network that can recognizes a "+" in a 3x3 grid of input pixels.

2 Axon Hilock Design

The axon hillock is a specialized part of the cell body (or soma) of a neuron that connects to the axon[2]. The axon hillock and initial segment have a number of specialized properties that make them capable of action potential generation, including adjacency to the axon and a much higher density of voltage-gated ion channels than the one found in the rest of the cell body[3].

2.1 Circuit Schematics

Here shows the schematics of an amplitude-sensitive axon hilock, which follows the idea of Hsu's dendritic circuit model[4].

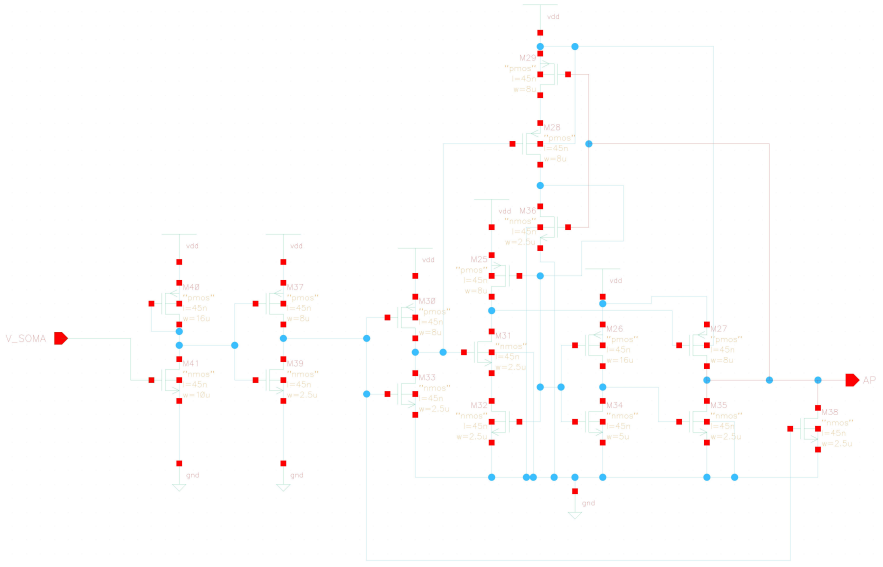

Figure 1: Schematics of Axon Hilock

2.2 Functionality

The functionality of the amplitude-sensitive axon hilock is shown below. When a input voltage is given with its amplitude as around 480mV, which is beyond the threshold, it will give an output spike with the amplitude as around 1V.

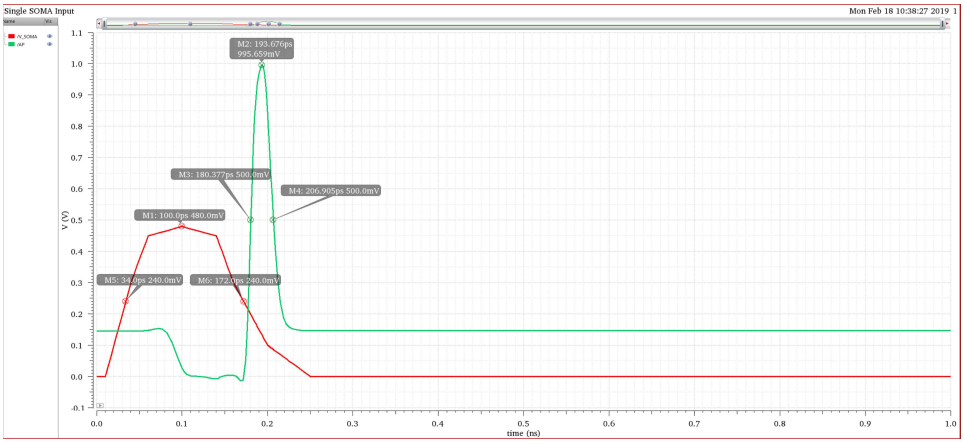

Figure 2: Functionality of Axon Hilock

3 Synapse Design

The synapse is one of the most important parts of a neuron. To simulate the operation of a neuron, we have to build these following parts: neurotransmitter action, membrane potentials, and ion pumps[5].

3.1 Circuit Schematics

Here shows the circuit schematics of a synapse, which follows BioRC biomimetic real-time cortex synapse[5].

3.2 Functionality

Here shows the functionality of the synapse. When a input spike with 1V amplitude is given, as the response, it will give an EPSP signal as the output, which has an amplitude around 200mV.

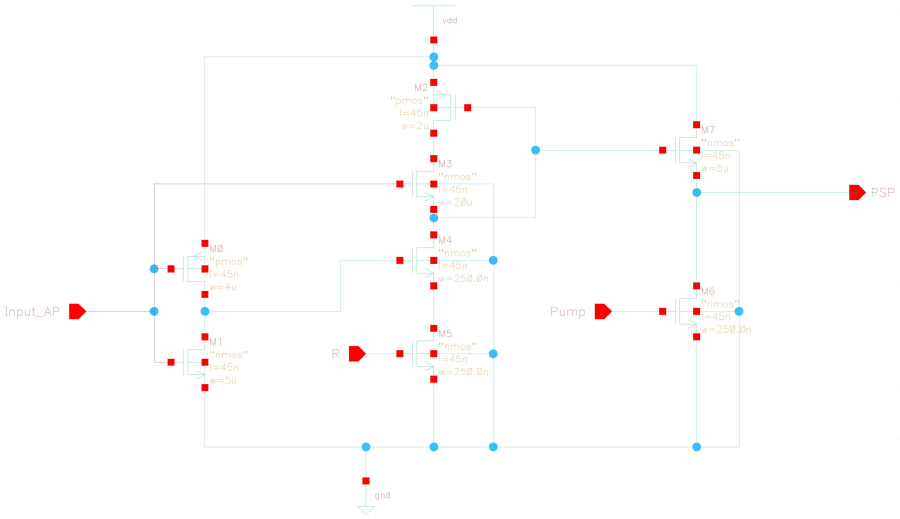

Figure 3: Schematics of Synapse

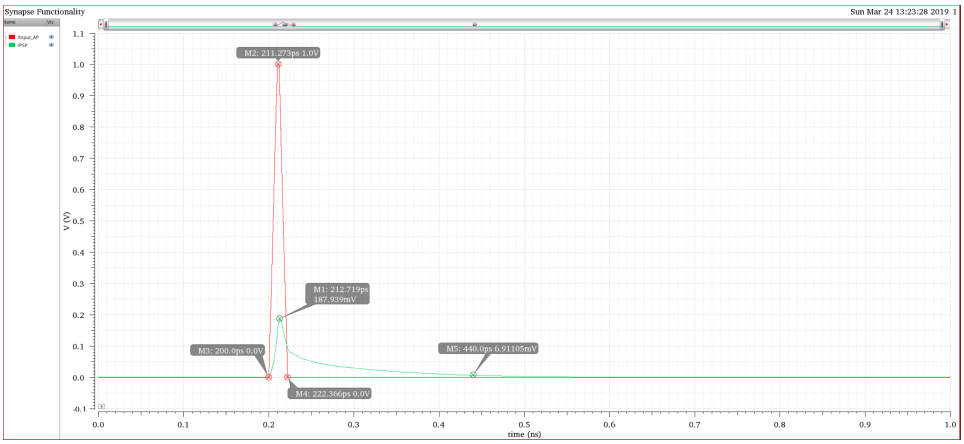

Figure 4: Functionality of Synapse

4 Logic Element Design

4.1 Singal Decision

Here is the most important part of this project. Firstly, we have to design how to decide whether it's a "bright" element or a "dark" one. Here for a "bright" element, it will stimulate an impulse to the synapse, which is a 1V spiking signal, while for a "dark" element, nothing will happen, there will be no impulse transmitted to the input of the synapse, therefore there will be no EPSP signal at the output.

4.2 Analog Adder Circuit Schematics

We have to design an analog adder to count how many "bright" elements and "dark" elements shown there. The function of an analog adder is to perform the voltage addition of two input analog voltage signals as the output. The subtractor has the similar function but do subtraction.

Here shows schematics of the analog adder circuit.

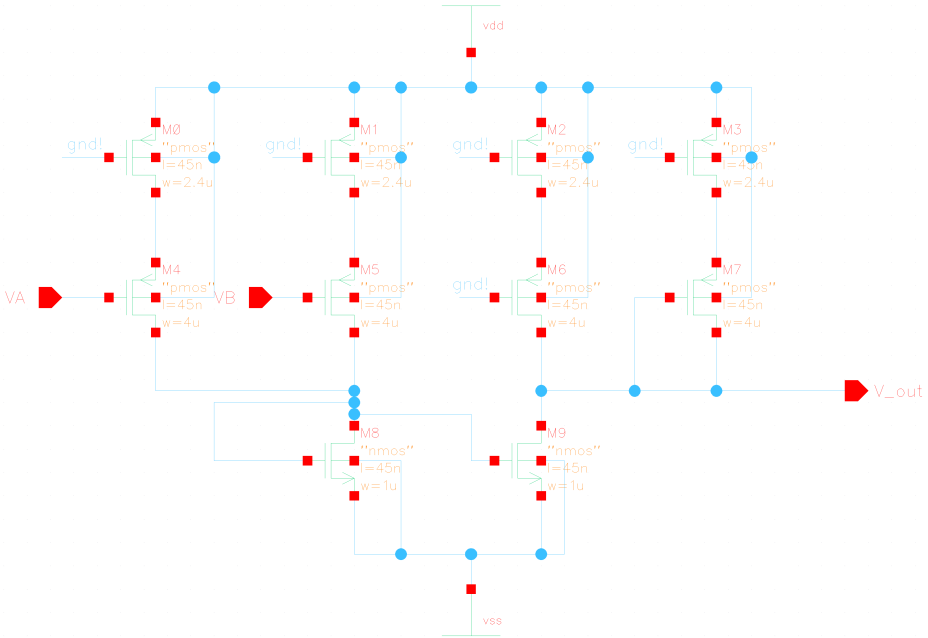

Figure 5: Schematics of Analog Adder

4.3 Logic Element

Here shows the general schematics of the logic element.

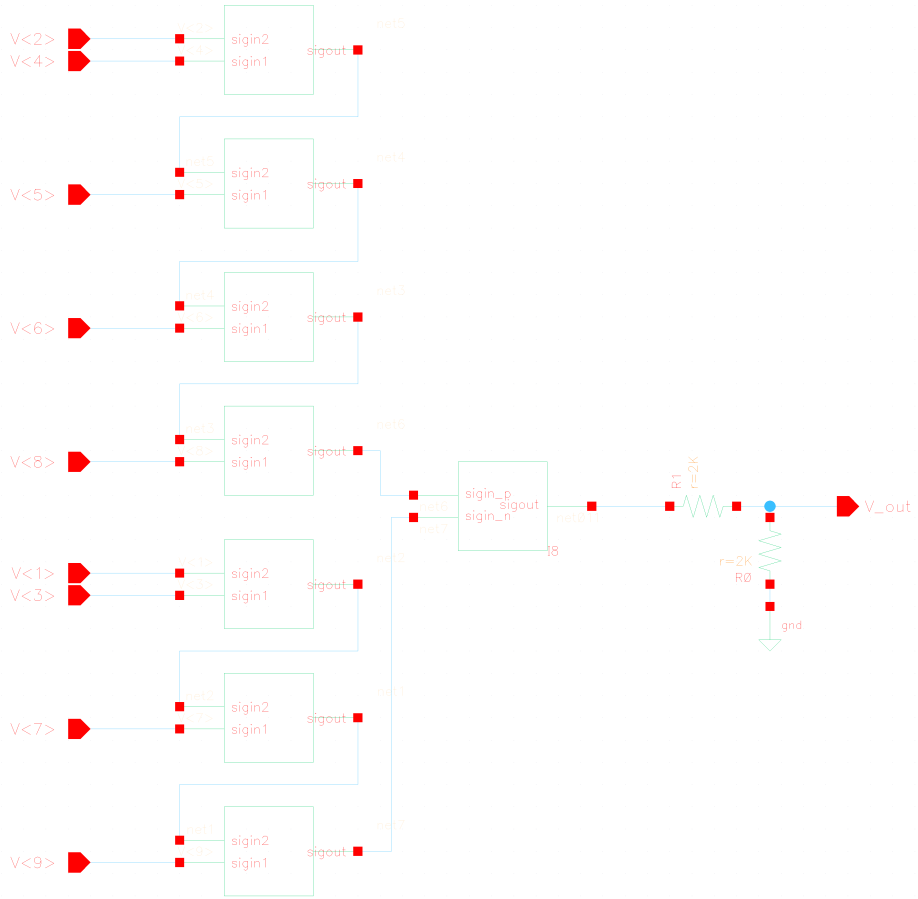

Figure 6: Schematics of Logic Element

In Figure 6, we can divide the circuit into two parts, first part is the voltage calculation, and second part is the voltage division.

For the voltage calculation, the upper four adders will calculate the sum of the input signals of V<2>, V<4>, V<5>, V<6> and V<8>, which is the "+" part of the 3x3 grid. And the lower three adders will do the sum of V<1>, V<3>, V<7> and V<9>, which is the rest part of the grid. And they will go through a subtractor and its output will be sent to the voltage divider part. The most tricky part is that when one of "+" element is not "bright", then the voltage addition of the upper part will not be high enough to stimulate the next stage. Or say if there is "bright" element on the side (say 1, 3, 7, 9), since they are in the subtraction part, the output voltage will also be decreased to the level that is not enough to stimulate the next stage. The sequence diagram is shown below.

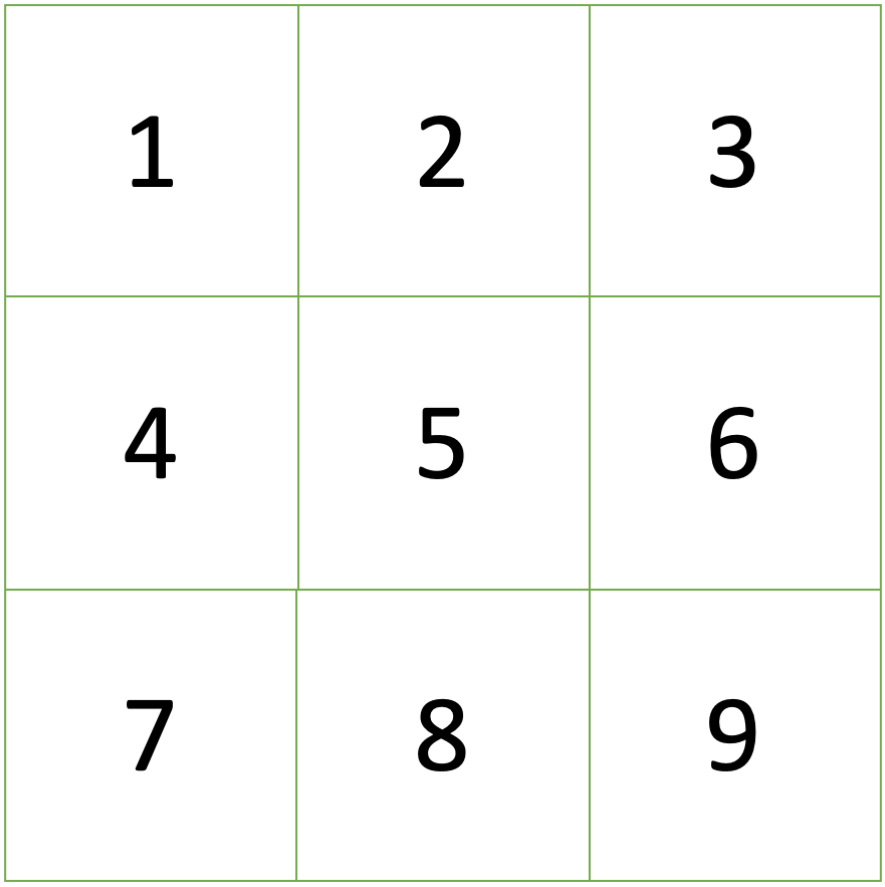

Figure 7: Sequence Diagram

The voltage division part is to help designing the final output voltage so

that the output voltage for "+" case is the only case that can stimulate the next stage.

5 Complete Circuit

5.1 Circuit Schematics

There gives the schematics of the complete circuit.

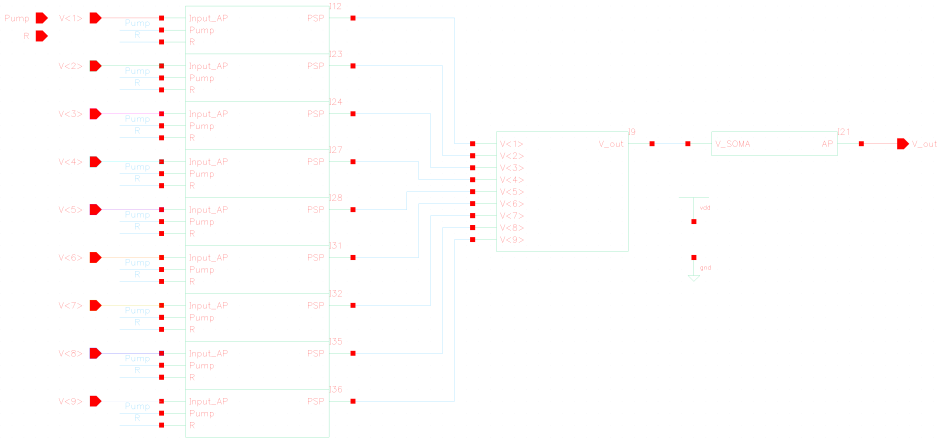

Figure 8: Schematics of Complete Circuit

The circuit contains three stages. First stage is the detection synapse, when there is a "bright" element, it will generate a EPSP singal, with an amplitude around 200mV. Second stage is the logic element stage, only when the input case is the "+" shaped bright elements, it can give a high enough output signal to the next stage. Third stage is the amplitude-sensitive axon hilock stage, only when the input voltage is higher than 0.5V, it will give a spiking signal output.

5.2 Functionality

Here shows three cases to prove the functionality of the circuit. First One is for there is only "+" region is bright, second one is that there is one more element outside the "+" region is also bright, third one is that all elements are bright.

5.2.1 "+" Shaped Bright Case

Here only V<2>, V<4>, V<5>, V<6> and V<8> are bright, which can give a pulse input while the others are all 0. We can see that in this case, the output

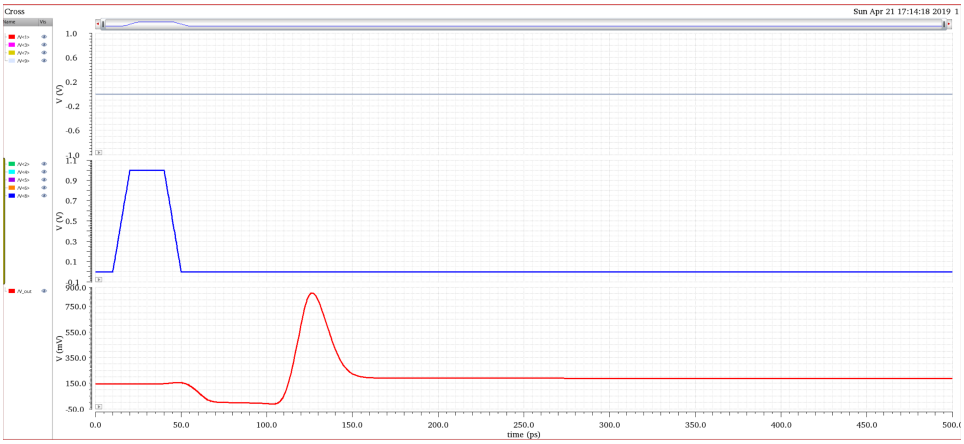

Figure 9: Simulation of "+" Shaped Bright Case

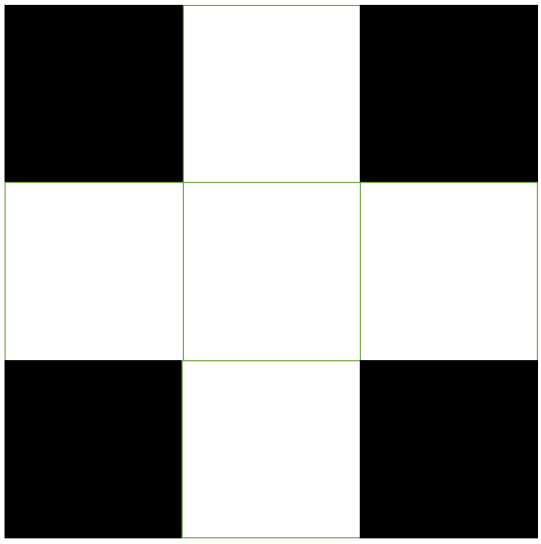

Figure 10: Configuration of "+" Shaped Bright Case

gives a spiking signal with an amplitude as around 900mV.

5.2.2 One Bright Side Element Case

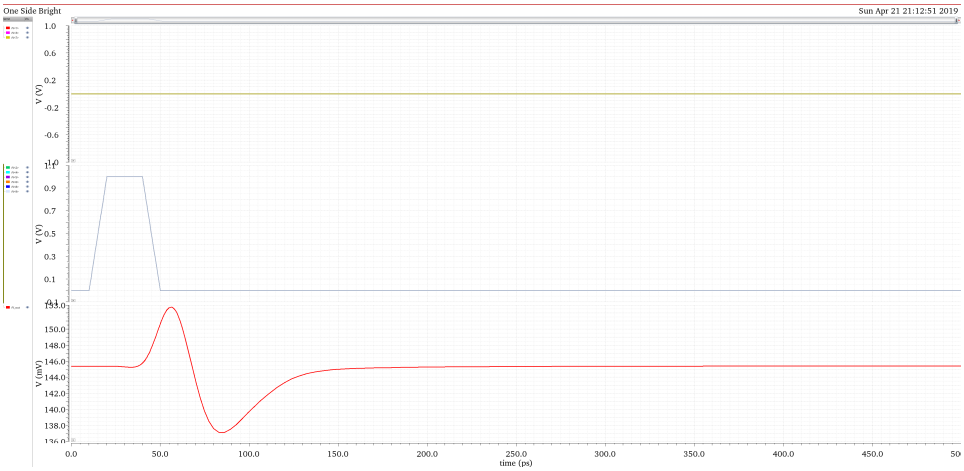

Figure 11: Simulation of One Bright Side Element Case

Here besides the "+" region, there is one more element is also bright, which is V<9>, and as a result, the output signal only gives a small glitch, which is almost the keep its normal value as around 150mV.

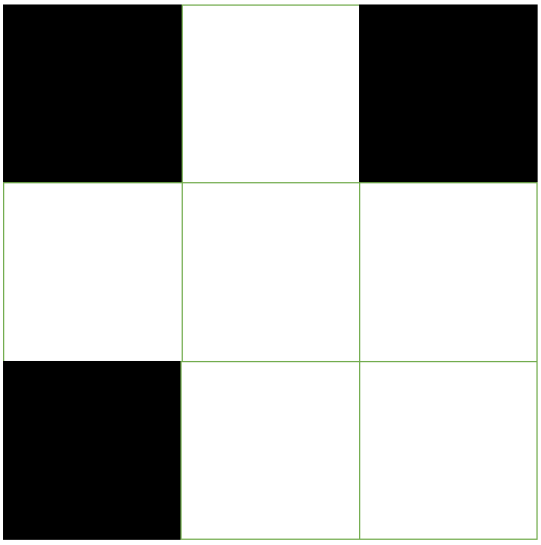

Figure 12: Configuration of One Bright Side Element Case

5.2.3 All Bright Case

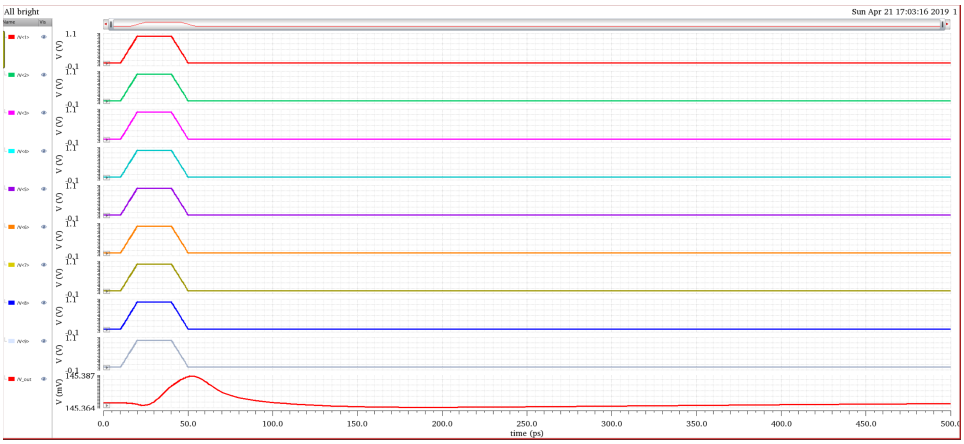

Figure 13: Simulation of All Bright Case

Similar to the previous case, when the inputs are all bright, the output doesn't give an pulse as well.

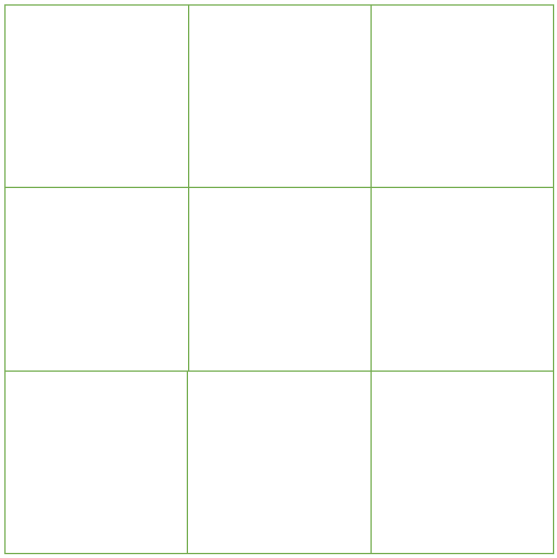

Figure 14: Configuration of All Bright Case

6 Conclusion

In this project, I designed the circuit that can perform border-ownership detection of the "+" shape. But actually, based on this concept, it can detect any shape as long as the criterion is given. One thing that need to be improved is that for a normal axon hilock output, its amplitude should be at 1V, which is the Vdd, but in this circuit, it was just 900mV, which lost about 100mV, which may cause some problem in future usage.

References

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