EE582 Spring 2019 Lab#2 Report

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Contents

1 Introduction

In biological neurons, the axon hillock is the neuronal spike initiation region. The axon hillock is a specialized part of the cell body (or soma) of a neuron that connects to the axon[1]. The axon hillock and initial segment have a number of specialized properties that make them capable of action potential generation, including adjacency to the axon and a much higher density of voltage-gated ion channels than the one found in the rest of the cell body[2].

For the operation principle of axon hillock, it is enriched with sodium and potassium channels that are responsible for generating and shaping the action potential (AP). A fast sodium influx followed by a slow potassium outward current, causes the membrane potential at the axon hillock to rise rapidly and return to resting potential when equilibrium between the inward and outward currents is reached[3][4].

Although it is generally believed that cortical neurons integrate their synaptic inputs and fire APs when the threshold is reached, some evidence has supported the theory that the threshold to fire an AP spike of cortical neurons in vivo depends on both the amplitude and the rate of membrane potential depolarization[5]. To make a basic and regular spiking model, I applied the Chih-Chieh Hsu's basic model to build the spiking circuit.

2 Design Concept

2.1 Parameters of MOSFET

Firstly, we will need to find out the parameters of the NMOS and the PMOS such as μC_{ox}, V_{th} and λ so that we can do hand calculation to find out the approximate designing value. Since the channel length modulation will effect these parameters, so we choose the minimum value of the channel length as 45nm, which is also one of the standard fabrication processes being used nowadays.

We applied the test circuit as Figure 1 to measure the properties of the MOSFETs (It is also used for NMOS testing). Table 1 shows the hand calculation result of V_{th}, μC_{ox} and λ of both NMOS and PMOS with $W = 30\mu m$ and $L = 45nm$.

Table 1: Parameter Extration of L=180nm, W=30μm Transistor

	V_{th} **(V)**	μC_{ox} **(mA/V^2)**	λ **(V^{-1})**	$V_{th,body}$ **(V)**
NMOS	0.390	0.280	0.86	0.440
PMOS	-0.370	0.036	-0.27	-0.450

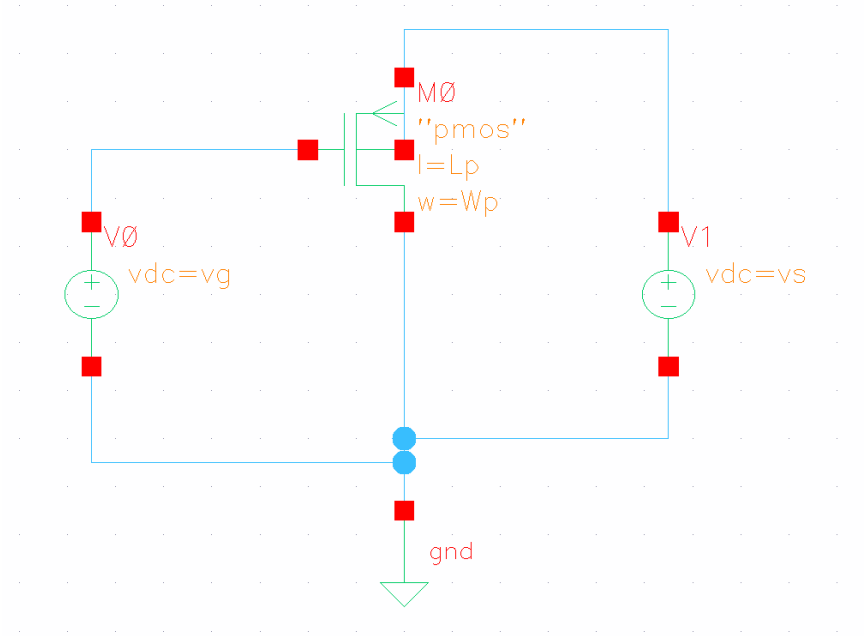

Figure 1: Parameter Test Circuit

2.2 Amplitude-Sensitive Axon Hillock Circuit

The circuit implementation of the axon hillock at the transistor level is shown in Figure 2[3].

The function of this circuit is that when the input V_{SOMA} is above a certain threshold, the output will generate a spike. The pull-up transistor (X8) models the fast inward sodium current while the pull-down transistor (X7) models the slow outward potassium current. To mimic a fast rising phase due to the rapid increase of the Na^+ (sodium) channel conductance and a slower falling phase due to the slow increase of the K^+ (potassium) channel, the strength of transistors X8 (PMOS) and X7 (NMOS) should be controlled[4].

The color-shaded segments mimic the activation and inactivation phases of the sodium and potassium channels as well as the delay time for the sequence of events that define the dynamics of an AP. First, when a input signal V_{SOMA} is given and its amplitude is larger then the threshold of the input NMOS, Na^+-activation segment (X1, X2) turns on Na^+ channels (X8) rapidly. Transistor X8 is set to be less resistive to mimic the fast rise in AP. After some delay, the voltage level of the output (AP) will reach a high level, then the Na^+-inactivation (X3) will turn off Na^+ channels. This portrays the gradual inactivation of Na^+ channels when the action potential reaches a

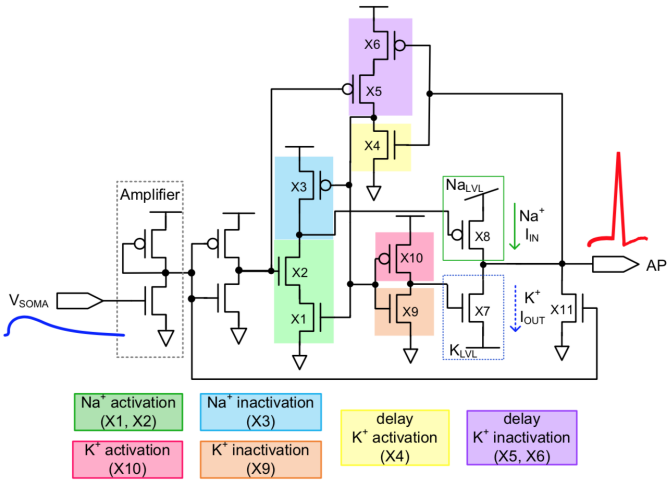

Figure 2: Amplitude-Sensitive Axon Hillock Circuit[3]

depolarizing state. K^+-activation (X10), after some more delay (X4), turns on K^+ channels. Transistor X10 is designed to be more resistive than X3 in order to mimic the biological behavior such that K^+-activation occurs a short period of time after Na^+-inactivation begins. Then K^+-inactivation (X9) will turn off K^+ channels after a longer delay (X5, X6). The delay is controlled by adjusting the strengths of transistors[3].

2.3 Sizing Strategy

To achieve the minimum performance of the circuit, say the fastest rising and falling time of the output spike, I applied all the MOSFETs as the channel length of 45nm.

For transistors X8 and X7, which model the Na^+ channel and the K^+ channel, the size of it will determine the speed of charge and discharge, which is exactly the rising and falling time. With larger channel width length ratio, it can achieve better performance of spikes. For this reason, I chose the channel width for the NMOS (X7) as 2.5μm, which is a decent value in sizing. And since the β ratio between PMOS and NMOS is around 3.5, I chose the PMOS as 8μm.

For transistor X4, which is the delay of the whole circuit. The function of this inverter is to make a delay after the Na^+ channel is turned on. To assure there is enough time to charge the output node, this delay is designed to be large enough. The size of X4 is designed as 2.5μm, which is large enough so that the output node can reach the highest value.

For transistors X10 and X9, which model the K^+ inactivation and the K^+ activation, they should be more resistive and work as a delay to some extent. The size of them are 16μm and 5μm.

For transistors X6 and X5, which is also a delay. Its function is to model the K^+ inactivation, which is the opposite to the function of X4. Also to make this delay larger, the size of the transistors should be decreased. Then both of them are sized as 8μm.

For transistors X3-X1, they and Na^+ inactivation and activation. The function of them are kind of like the functin of X4 and X6, X5. The sizes of them are 8μm for PMOS and 2.5μm for NMOS.

For transistor X11, it's just a path to discharge, its size is 2.5μm. For the rest transistors, they work as the driving inverters. The size of it is 8μm for PMOS and 2.5μm for NMOS. And for the amplification circuit, since we need a higher sensitivity and less responding time, the size of the PMOS is 16μm and NMOS is 10μm.

Table 2: Transistor Sizing

Name	**L (nm)**	**W (μm)**	**Name**	**L (nm)**	**W (μm)**
X1	45	2.5	X2	45	2.5
X3	45	8	X4	45	2.5
X5	45	8	X6	45	8
X7	45	2.5	X8	45	8
X9	45	5	X10	45	16
X11	45	2.5			

Table 2 shows the parameter setting of all the important transistors in the circuit.

3 Simulation Result&Conclusion

3.1 Circuit Schematics

Figure 3 shows the schematics of the spiking circuit. The sizing details are also shown in the figure.

3.2 Simulation Result

For simulation, I tested three kinds of input signal. First one is the single SOMA signal, second one is a bunch of SOMA signals and third one is a SOMA signal with some fluctuations. All the simulation result are shown in next three subsections. Since the threshold voltage with body effect of the

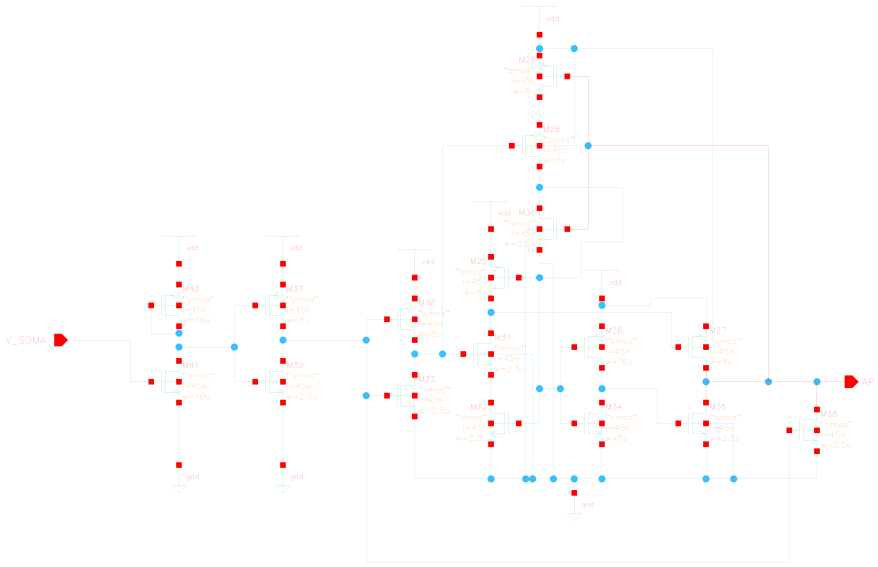

Figure 3: Circuit Schematics

NMOS is around 0.45V, I chose 0.48V as the apex value of the input singal V_{SOMA}.

3.2.1 Single SOMA Signal Input

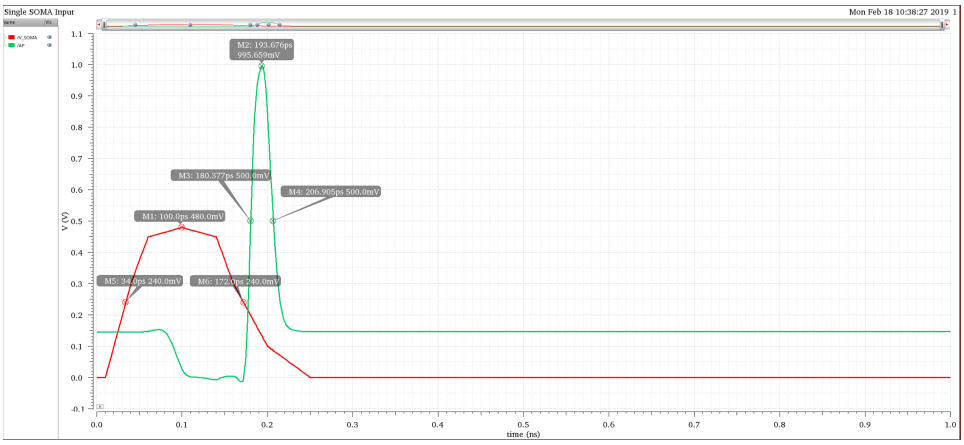

Figure 4: Simulation with Single SOMA Signal Input

Figure 4 shows the simulation result with a single SOMA input. The amplitude of the SOMA signal is 480mV, and the output spike is 1V, which is twice larger than the input SOMA signal. The time width of the SOMA is

around 140ps, and the time width of the output spike is about 25ps, which is also within the expectation.

3.2.2 Multiple SOMA Signal Input

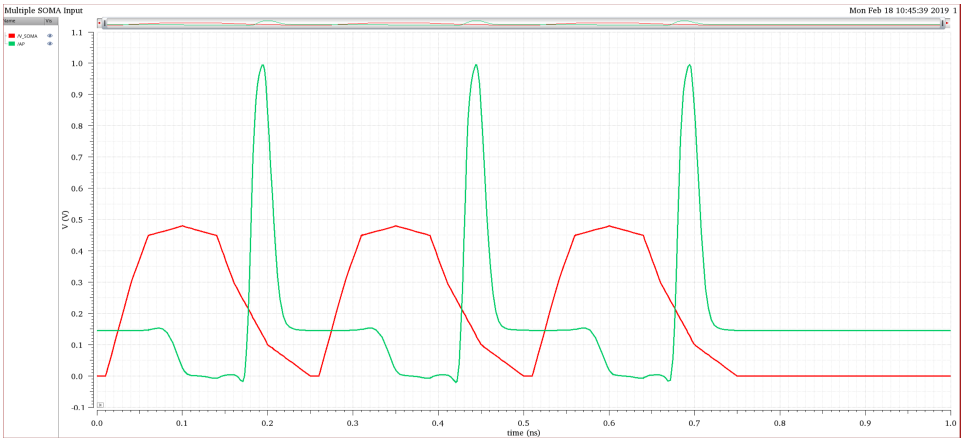

Figure 5: Simulation with Multiple SOMA Signal Input

Figure 5 shows the simulation result with multiple SOMA inputs. The circuit will respond to each SOMA signal and generate a spike as the same amplitude and time width in the single input case.

3.2.3 SOMA Signal Input with Fluctuation

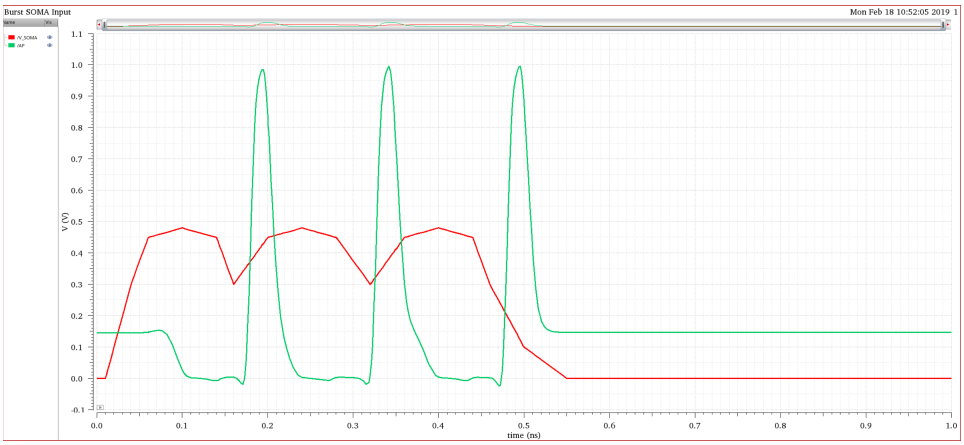

Figure 6: Simulation with SOMA Signal Input with Fluctuation

Figure 6 shows the simulation result with a SOMA with some fluctuation. The input singal will drop below 300mV but not drop to 0 and go op again to

the apex as 480mV and repeat it. The simulation shows that the circuit will also generate spikes that corresponding to each rising of the input signal.

References

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